SPACE VECTOR MODULATION OF DYNAMIC VOLTAGE RESTORER TO IMPROVE POWER QUALITY

A thesis submitted
in partial fulfillment of requirements
for the degree of

Master of Technology

by

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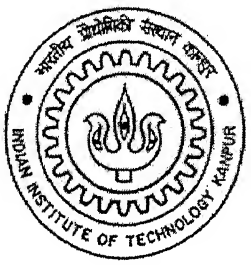

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JUNE 2005

CERTIFICATE

This is to certify that the work contained in this thesis entitled **"Space Vector Modulation of Dynamic Voltage Restorer to Improve Power Quality"**, by **Bhaumik B. Sherdiwala**, has been carried out under our supervision and this work has not been submitted elsewhere for a degree.

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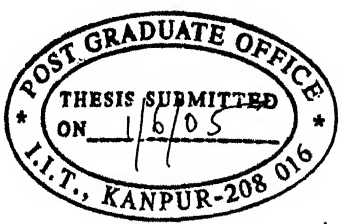

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Dedicated to my parents,

my uncle and aunty

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ABSTRACT

Various types of voltage disturbances occur in a power distribution system. These disturbances may be due to voltage sag/swell, unbalance, distortion, momentary interruption, flicker etc. These disturbances may be unacceptable to most customers. Office automation, process automation, medical and communication equipment used in everyday life are sensitive to such voltage disturbances. If these disturbances are not properly mitigated, they can be the cause of equipment breakdown or mal-operation resulting in equipment damage or production loss. Dynamic Voltage Restorer (DVR) is a compensating type custom power device that protects sensitive loads from all kinds of supply side disturbances. The DVR is realized using a solid-state DC to AC switching power converter (inverter) that injects voltages of required magnitude, phase and frequency in series with the distribution feeder such that the load voltages become balanced sinusoidal. Voltage source inverters (VSI) are used to inject voltages effectively and efficiently.

In the present work, DVR operation for voltage sag mitigation has been discussed. Three different VSI topologies viz., two-level three-leg VSI, two-level four-leg VSI and three-level diode clamped VSI have been used to realize the DVR separately. Space Vector Modulation (SVM) technique has been used for all the three VSIs. Important issues for SVM, such as definition of voltage space vectors, identification of nearest vectors, calculation of switching time and switching sequences have been addressed. Simulation results for the DVR operation during voltage sag have been presented and performance evaluation of DVR using different VSIs have been examined.

Key Words: - Dynamic Voltage Restorer, Space Vector Modulation.

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CHAPTER 1

INTRODUCTION

Various types of voltage disturbances can occur in a distribution system due to faults or badly behaved loads. These disturbances include momentary interruption, distortion, over voltage/under voltage, sag/swell, flicker, etc. This may be quite unacceptable to most customers. Office automation, process automation, medical and communication equipment used in everyday life are sensitive to such voltage disturbances. If these disturbances are not properly mitigated, they can be the cause of equipment breakdown or mal-operation resulting in equipment damage or production loss.

Dynamic Voltage Restorer (DVR) is a custom power device for the protection of sensitive loads from supply side disturbances. The DVR is made of a solid-state dc to ac switching power converter (inverter) that injects voltages of required magnitude, phase and frequency in series with the line so that the load voltages become balanced sinusoidal. Voltage source inverters (VSI) can be used for this purpose to inject voltages effectively and efficiently.

The use of pulse-width modulation (PWM) with high switching frequency ensures that VSI generates a smooth voltage waveform, with distortion components shifted to higher frequency band. Harmonics can then be canceled by using small passive filters. There are different PWM strategies to modulate VSIs. The most popular and widely used modulation strategy is sinusoidal pulse width modulation (SPWM). Another strategy for VSI modulation is the space vector modulation (SVM).

1.1 Dynamic Voltage Restorer

A dynamic voltage restorer (DVR) is a custom power device that is suitable for protecting sensitive loads from supply side disturbances like voltage sags [1] and distortion. It is basically a series compensator, which injects voltages of required magnitude, phase

and frequency in series with the line. Issues related with DVR are: filter structure, VSI configuration and dc source for the VSI.

Voltages are injected in series with the line using a VSI through a filter and an isolation transformer. The transformers not only reduce the voltage requirement of the inverters but also provide isolation between the inverter phases. This prevents the dc battery or dc storage capacitor from being shorted through switches in different phases of inverter. The filter is needed to remove higher order harmonics present in the VSI output voltage [2]. It can be placed on the inverter side or on the feeder side of the isolation transformer. Further, filters used for DVR can be classified as Capacitor filter and LC filter.

Various VSI configurations can be used for DVRs used in various system configurations. For example, a three-leg VSI with star point of transformer primary kept isolated, can be used to compensate for balanced sag/swell. A four-leg VSI with star point of transformer primary connected to the middle of the fourth leg of VSI, can be used to compensate for balanced as well as unbalanced sag/swell.

dc supply to the VSI can be provided in various ways. One option is to use a dc battery. Other option is to use dc capacitors, which will be charged by another energy source like a rectifier supplied from the system itself.

Depending on the system and requirement on the load side, suitable choices have to be made regarding VSI configuration, dc supply for VSI, modulation strategy for VSI and filter structure.

1.2 Space Vector Modulation

VSIs have been used to synthesize ac voltage waveforms in several applications, such as Uninterruptible Power Supplies (UPSs), motor drives and active filters. To generate the inverter output voltages, several modulation strategies, differing in concept and performance, have been developed. One such voltage modulation strategy is the space vector modulation (SVM).

The space vector PWM is based on the space vector representation of voltages in the complex plane. The basic concept of the SVM is to get required reference voltage as combination of two or more inverter voltage vectors. Different VSIs have their own voltage

vector set. The two-level three-leg VSI has eight vectors in 2-dimensional plane, while two-level four-leg VSI has sixteen vectors in 3-dimensional space. Three-level VSI has twenty-seven vectors in 2-dimensional plane. As the number of levels for an inverter increases, number of voltage space vectors also increases and it becomes difficult to implement SVM for such cases. This drawback can be overcome by converting multilevel SVM problem to two-level SVM problem.

The first step in the implementation of SVM is to recognize its voltage space vectors and their distribution in the space. Second step is to select the vectors most suitable for producing the reference voltage. Next step is to calculate switching time for each voltage vector and the final step is to decide the switching sequence. In fact, the main benefit of SVM is the explicit identification of pulse placement as an additional degree of freedom that can be exploited to achieve harmonic performance gains. Another advantage of SVM is that it can be easily implemented on digital processors.

1.3 Thesis Organization

Chapter 1 gives the general introduction of SVM and DVR.

In Chapter 2, SVM techniques for following three types of VSIs are discussed,

(i) Two-level three-leg VSI

(ii) Two-level four-leg VSI

(iii) Three-level diode clamped VSI

For two-level four-leg VSI a three-dimensional SVM is discussed. For three-level diode-clamped VSI, a technique is discussed in which the three-level SVM problem is reduced to that of a two-level SVM. Simulation results for all these VSIs with RL load are presented.

Chapter 3 discusses the DVR operation during voltage sags with above-mentioned VSIs. In case of DVR using two-level three-leg VSI and three-level diode clamped VSI, the star point of the transformer primary is kept isolated. In case of DVR using two-level four-leg VSI the star point of the transformer primary is connected to the middle point of the fourth leg. The DVR supported by dc battery and rectifier supported DVR are discussed. Simulation results for these systems are presented and their performances are compared.

Chapter 4 gives the conclusions and scope for future work.

CHAPTER 2

SPACE VECTOR MODULATION FOR VOLTAGE SOURCE INVERTER CONFIGURATIONS

Voltage source inverters have been used to synthesize ac voltage waveforms in several applications, such as Uninterruptible Power Supplies (UPSs), motor drives and active filters. As a result, a number of inverter topologies have been developed ranging from single-phase half-bridge to three-phase four-leg inverters. To generate the inverter output voltages, several modulation strategies, differing in concept and performance, have been developed [3]. Among these strategies, the sinusoidal pulse width modulation (SPWM) has been extensively used, because it improves the harmonic spectrum of the inverter by moving the voltage harmonic component to higher frequencies [4].

Another voltage modulation strategy is space vector modulation (SVM). SVM techniques have been increasingly used because of the following advantages:

- SVM techniques can reduce commutation losses and/or the harmonic content of output voltage.
- Higher amplitude modulation indexes can be obtained compared to conventional SPWM techniques [5-6].
- SVM techniques can be easily implemented on digital processors [7-8].

In general following steps can be identified to implement the SVM for voltage source inverters.

1. Identification of voltage space vectors for a particular VSI.
2. Identification of the nearest voltage space vectors.
3. Calculation of switching time.
4. Determination of switching sequence.

In this chapter, space vector modulation techniques for two-level three-leg, two-level four-leg and three-level diode clamped voltage source inverter configuration will be discussed.

2.1 SVM for Two-Level Three-Leg VSI

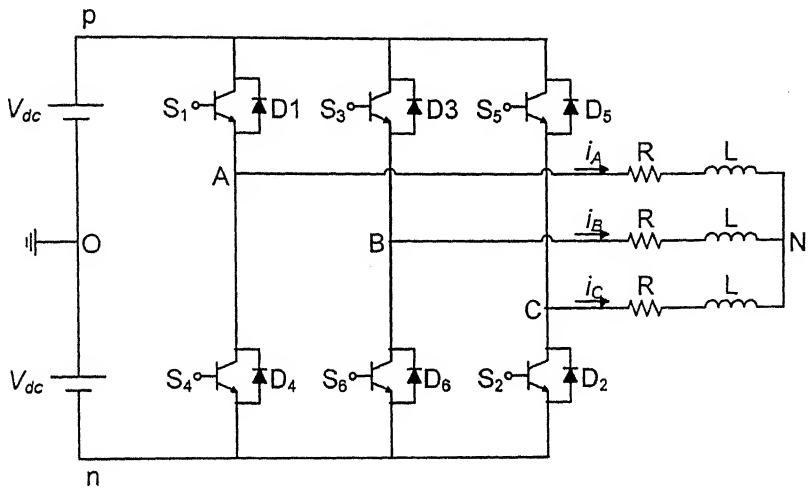


Fig. 2.1 Two-level three-leg VSI with balanced RL load.

The two-level three-leg voltage source inverter is shown in Fig. 2.1. It consists of 6 switches (S_1 to S_6) with anti-parallel diodes (D_1 to D_6). There are two switches in each leg. The dc source is divided into two parts with ground as the center point, O. The three-phase output is provided at points A, B and C. This inverter provides two levels of voltages $+V_{dc}$ and $-V_{dc}$ at the output terminals A, B and C with respect to the center point of dc source, O.

2.1.1 Voltage Space Vectors

The pole voltages can be expressed as

$$v_{AO} = m_A * V_{dc} \tag{2.1}$$

$$v_{BO} = m_B * V_{dc} \tag{2.2}$$

$$v_{CO} = m_C * V_{dc} \tag{2.3}$$

where, m_A, m_B, and m_C are the switching states for the three legs of the inverter.

The output of each of the three states can be defined as '1' or '−1' depending on which of the two switches in a leg is ON. If upper switch in phase A, S_1 is ON then

$m_A = 1$ and if bottom switch S_4 is ON then $m_A = -1$. (Two switches in a single leg cannot be turned ON simultaneously to avoid short circuit of the dc source). The same notation applies to phase legs B and C.

If v_{NO} is the voltage from load neutral to the center point of dc source, we have

$$v_{AO} = v_{AN} + v_{NO} \tag{2.4}$$

$$v_{BO} = v_{BN} + v_{NO} \tag{2.5}$$

$$v_{CO} = v_{CN} + v_{NO} \tag{2.6}$$

If the neutral point, N, is kept isolated, sum of output currents is zero. For balanced load this implies $v_{AN} + v_{BN} + v_{CN} = 0$. Therefore from (2.4), (2.5) and (2.6),

$$v_{NO} = \frac{1}{3} * (v_{AO} + v_{BO} + v_{CO}) \tag{2.7}$$

Using (2.1) to (2.7), the phase voltages can now be expressed as

$$v_{AN} = \frac{V_{dc}}{3} * (2m_A - m_B - m_C) \tag{2.8}$$

$$v_{BN} = \frac{V_{dc}}{3} * (-m_A + 2m_B - m_C) \tag{2.9}$$

$$v_{CN} = \frac{V_{dc}}{3} * (-m_A - m_B + 2m_C) \tag{2.10}$$

As switching states m_A, m_B and m_C are independent and as there are only two possible values for each switching state, there are $2^3 = 8$ switching combinations. So we have 8 possible values for pole voltages and phase voltages as shown in Table 2.1.

The complex pole voltage vector can be defined as

$$\overline{V} = V_\alpha + jV_\beta = \frac{2}{3}\left(V_{AN} + aV_{BN} + a^2V_{CN}\right) \tag{2.11}$$

where, $a = e^{j\frac{2\pi}{3}}$.

The 8 voltage values give voltage vectors distributed at different angles in the 2-D α-β plane as shown in Fig. 2.2. Two of these vectors ($\overline{SV_0}$ and $\overline{SV_7}$) are a short circuit of

the output while the remaining six vectors ($\overline{SV_1}$ to $\overline{SV_6}$) produce active voltages. These six active vectors have phase difference of 60° from each other.

The magnitude of each of the six active vectors is,

$$V_m = \frac{4}{3} V_{dc} \tag{2.12}$$

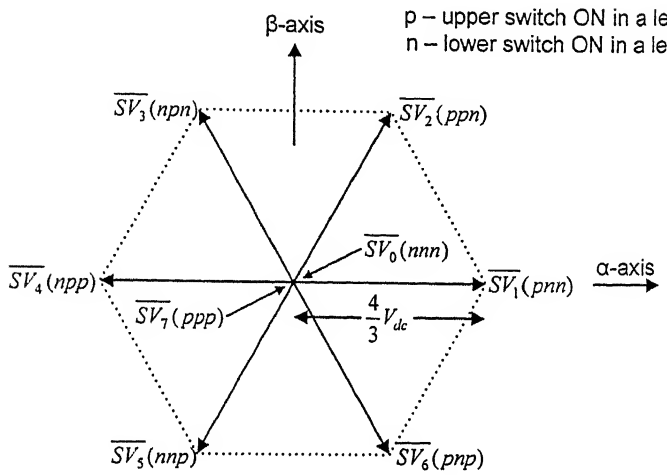


Fig. 2.2 Eight possible stationary vectors in 2-D α-β plane for a two-level three-leg VSI.

TABLE 2.1

Pole voltages, phase voltages and voltage vectors for two-level three-leg VSI.

m_A	m_B	m_C	v_{AO}	v_{BO}	v_{CO}	v_{AN}	v_{BN}	v_{CN}	$\lvert V\rvert$	$\angle V$	Voltage vector
−1	−1	−1	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$	0	0	0	0	0°	$\overline{SV_0}$
−1	−1	1	$-V_{dc}$	$-V_{dc}$	V_{dc}	$-\frac{2}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	$\frac{4}{3}V_{dc}$	$\frac{4}{3}V_{dc}$	240°	$\overline{SV_5}$
−1	1	−1	$-V_{dc}$	V_{dc}	$-V_{dc}$	$-\frac{2}{3}V_{dc}$	$\frac{4}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	$\frac{4}{3}V_{dc}$	120°	$\overline{SV_3}$
−1	1	1	$-V_{dc}$	V_{dc}	V_{dc}	$-\frac{4}{3}V_{dc}$	$\frac{2}{3}V_{dc}$	$\frac{2}{3}V_{dc}$	$\frac{4}{3}V_{dc}$	180°	$\overline{SV_4}$
1	−1	−1	V_{dc}	$-V_{dc}$	$-V_{dc}$	$\frac{4}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	$\frac{4}{3}V_{dc}$	0°	$\overline{SV_1}$
1	−1	1	V_{dc}	$-V_{dc}$	V_{dc}	$\frac{2}{3}V_{dc}$	$-\frac{4}{3}V_{dc}$	$\frac{2}{3}V_{dc}$	$\frac{4}{3}V_{dc}$	300°	$\overline{SV_6}$
1	1	−1	V_{dc}	V_{dc}	$-V_{dc}$	$\frac{2}{3}V_{dc}$	$\frac{2}{3}V_{dc}$	$-\frac{4}{3}V_{dc}$	$\frac{4}{3}V_{dc}$	60°	$\overline{SV_2}$
1	1	1	V_{dc}	V_{dc}	V_{dc}	0	0	0	0	0°	$\overline{SV_7}$

2.1.2 Generation of Reference Voltage Vector

A target reference voltage vector $\overline{V_{ref}}$ can be synthesized using three phase reference voltages. Let three phase reference voltages be v_{aref}, v_{bref} and v_{cref}. These reference voltages are sampled at frequency $F_S = \frac{1}{T_S}$, where T_S is the carrier interval. Then we can convert these three-phase voltages into a vector (2.11), where equivalent two-phase components are,

$$\begin{bmatrix} v_{\alpha ref} \\ v_{\beta ref} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{aref} \\ v_{bref} \\ v_{cref} \end{bmatrix} \tag{2.13}$$

Using these two-phase voltages, we can calculate the magnitude and angle of the target reference voltage vector as

$$V_{ref} = \sqrt{v_{\alpha ref}^{\ 2} + v_{\beta ref}^{\ 2}} \tag{2.14}$$

$$\theta_{ref} = \tan^{-1} \frac{v_{\beta ref}}{v_{\alpha ref}} \tag{2.15}$$

2.1.3 Identification of the Nearest Voltage Space Vectors

It can be seen from Fig. 2.2 that tips of vectors in 2-D α-β plane lie on a hexagon (shown dotted). The hexagon can be divided into six sextants separated by the six active voltage space vectors. Once the reference vector has been found the next step is to find the sextant in which this vector lies. Depending on the value of θ_{ref} one of the six sextants can be selected. The two active vectors corresponding to this sextant should be used to produce required reference voltage vector along with the two zero vectors. It should be noted that the reference voltage vector can be generated using any of the six active vectors and two zero vectors, but intuitively it is easy to see that the two nearest vectors would give optimum results.

2.1.4 Calculation of Switching Time

Having identified the nearest stationary vectors, at any point in time, the target output voltage vector $\overline{V_{ref}}$ can be formed by the summation of a number of these space vectors within one carrier period T_S [9]. This is shown in Fig. 2.3 for a target phasor in the first 60° segment of the plane.

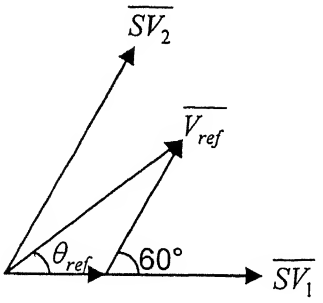


Fig. 2.3 Creation of an arbitrary output target phasor by the geometrical summation of the two nearest space vectors.

The geometric summation shown in Fig. 2.3 can be expressed mathematically as

$$\overline{V_{ref}} = V_{ref}\angle\theta_{ref} = \frac{T_1}{T_S}\overline{V_1} + \frac{T_2}{T_S}\overline{V_2} \tag{2.16}$$

for each carrier period of T_S, where T_1 is the time for which space vector $\overline{SV_1}$ is selected, and T_2 is the time for which space vector $\overline{SV_2}$ is selected.

(2.16) can be expressed as

$$V_{ref}\left(\cos\theta_{ref} + j\sin\theta_{ref}\right) = \frac{T_1}{T_S}V_m + \frac{T_2}{T_S}V_m\left(\cos 60° + j\sin 60°\right) \tag{2.17}$$

Equating real and imaginary components gives the solution of

$$T_1 = \frac{V_{ref}\sin(60° - \theta_{ref})}{V_m \sin 60°}T_S \qquad (\textit{Active time for } \overline{SV_1}) \tag{2.18}$$

$$T_2 = \frac{V_{ref}\sin(\theta_{ref})}{V_m \sin 60°}T_S \qquad (\textit{Active time for } \overline{SV_2}) \tag{2.19}$$

Now, the time for zero space vectors can be found out as,

$$T_Z = T_S - T_1 - T_2 \tag{2.20}$$

Here T_Z is the time for zero space vectors. Balance of the carrier period is made up of any combination of the zero space vectors $\overline{SV_0}$ and $\overline{SV_7}$. However, so far no rationale has been identified for selecting a particular combination of the two zero space vectors (although equal intervals for $\overline{SV_0}$ and $\overline{SV_7}$ are common). This freedom of choice allows the placement of the space vectors to be varied anywhere within the carrier period, which is the basis of most of the various space vector modulation alternatives that have been reported in the literature.

2.1.5 Switching Sequence

For SVM, the zero space vector positions are left undefined, and there is an opportunity to explore possible harmonic benefits by manipulating the zero pulse placements [10]. Here the switching sequence for the first sextant of the space vector phasor space is described for three different schemes. A similar sequence is readily established for the other five sextants using the two nearest space vector components for each sextant. Fig. 2.4 shows the pulse pattern in the first sextant for all the three schemes.

2.1.5.1 Scheme 1: Active Space Vector Pulses Centered at the Middle of the Half-Carrier Period

The conventional SVM implementation centers the active space vectors in each half-carrier period, and splits the remaining zero space vector time equally between $\overline{SV_0}$ and $\overline{SV_7}$. This creates a space vector sequence (for $0 \le \theta_{ref} \le \frac{\pi}{3}$) of:

$$\underbrace{\overline{SV_0} \rightarrow \overline{SV_1} \rightarrow \overline{SV_2} \rightarrow \overline{SV_7}}_{\frac{T_S}{2}} \rightarrow \underbrace{\overline{SV_7} \rightarrow \overline{SV_2} \rightarrow \overline{SV_1} \rightarrow \overline{SV_0}}_{\frac{T_S}{2}} \tag{2.21}$$

It should be noted from (2.21) that the sequence of space vectors reverses over a complete carrier interval. Further, the zero space vectors $\overline{SV_0}$ and $\overline{SV_7}$ are placed in such a way that transition from one state to another makes only one switch to change its state. The

sequence of (2.21) can be implemented with the active space vector periods T_1 and T_2 recalculated every half-carrier period or once per entire carrier period T_S.

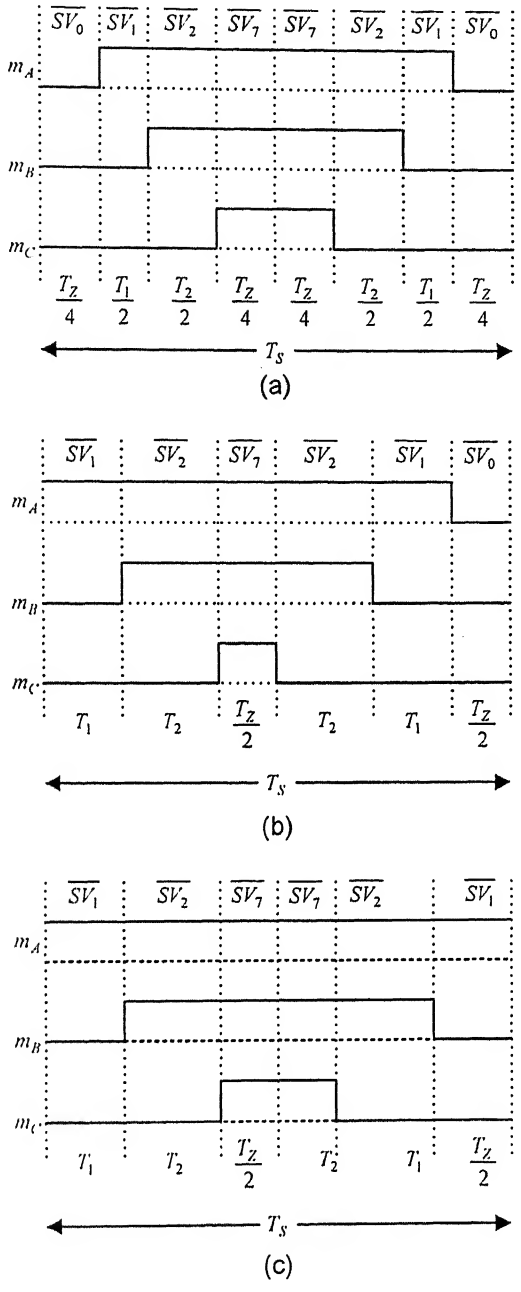


Fig. 2.4 Pulse pattern of space vector modulation in the first sextant, $0 \le \theta_{ref} \le \frac{\pi}{3}$ with (a) active pulses centered in the middle of the half-carrier period, (b) high quality pulses, (c) high efficiency pulses.

2.1.5.2 Scheme 2: High Quality SVM Pulses [11]

In this scheme only one of the two zero vectors is used in each half-carrier period. The two zero vectors $\overline{SV_0}$ and $\overline{SV_7}$ are placed at the end of each alternate half-carrier period. Particular zero vector for each half-carrier period is chosen such that transition from one state to another makes only one switch to change its state. For the same purpose, sequence of active space vectors is reversed over a complete cycle. The resulting space vector sequence (for $0 \le \theta_{ref} \le \frac{\pi}{3}$) is:

$$\begin{array}{l} \overline{SV_1} \rightarrow \overline{SV_2} \rightarrow \overline{SV_7} \rightarrow \overline{SV_2} \rightarrow \overline{SV_1} \rightarrow \overline{SV_0} \\ \left|\longleftarrow \frac{T_S}{2} \longrightarrow\right\|\left\longleftarrow \frac{T_S}{2} \longrightarrow\right| \end{array} \qquad (2.22)$$

2.1.5.3 Scheme 3: High Efficiency SVM Pulses

In this scheme only one of the two zero vectors is used in each carrier period. One of the two zero space vectors $\overline{SV_Z} = \overline{SV_0} / \overline{SV_7}$ is placed at the end and at the start of each alternating half-carrier period. Particular zero vector for each carrier period is chosen such that transition from one state to another makes only one switch to change its state. The resulting space vector sequence (for $0 \le \theta_{ref} \le \frac{\pi}{3}$) is:

$$\begin{array}{l} \overline{SV_1} \rightarrow \overline{SV_2} \rightarrow \overline{SV_Z} \rightarrow \overline{SV_Z} \rightarrow \overline{SV_2} \rightarrow \overline{SV_1} \\ \left|\longleftarrow \frac{T_S}{2} \longrightarrow\right\|\left\longleftarrow \frac{T_S}{2} \longrightarrow\right| \end{array} \qquad (2.23)$$

2.1.6 Amplitude Modulation Index

Since $0 \le T_1, T_2 \le T_S$, the maximum possible magnitude for $\overline{V_{ref}}$ is V_m, which can occur at $\theta_{ref} = 0$ *or* $60°$. However, a further constraint is that the sum of the active times for the two space vectors obviously cannot exceed the carrier period, i.e., $T_1 + T_2 \le T_S$. From simple geometry, the limiting case for this occurs at $\theta_{ref} = 30°$, which means that

$$\frac{T_1 + T_2}{T_S} = \frac{2V_{ref} \sin 30°}{V_m \sin 60°} \leq 1 \tag{2.24}$$

and this relationship constrains the maximum possible magnitude of $\overline{V_{ref}}$ to

$$V_{ref} = \frac{\sqrt{3}}{2} V_m = \frac{2}{\sqrt{3}} V_{dc} \tag{2.25}$$

Since V_{ref} is the magnitude of the output phase voltage, the maximum possible *l-l* output voltage using SVM must equal

$$V_{l-l} = \sqrt{3} V_{ref} = 2V_{dc} \tag{2.26}$$

Thus there is an increase of $\frac{2}{\sqrt{3}} \approx 1.15$ in amplitude modulation index for SVM compared to sinusoidal pulse width modulation (SPWM). So, for the same VSI and with same dc supply, maximum output voltage level achieved by SVM is 15% more compared to SPWM.

2.1.7 Simulation Results

System parameters chosen for simulation of two-level three-leg VSI with balanced RL load as shown in Fig. 2.1 are given in Table 2.2. The output line-line voltage, phase voltage, and reference voltage are shown in Fig. 2.5 for scheme 1 of switching sequence as discussed in Section 2.1.5.1. Fig. 2.6 shows the phase currents and Fig. 2.7 shows the frequency components in the line and pole voltages. It should be noted that while line voltage does not contain lower order harmonics, the pole voltage contains third harmonic of 20.19%.

TABLE 2.2

System Parameters for two-level three-leg VSI with balanced RL load.

System Parameters	Values of Parameters
dc Voltage	$2V_{dc}$ = 400 Volts
Load Resistor	R = 1.0 Ω
Load Inductor	L = 0.01 H
Sampling Frequency	F_S = 2000 Hz

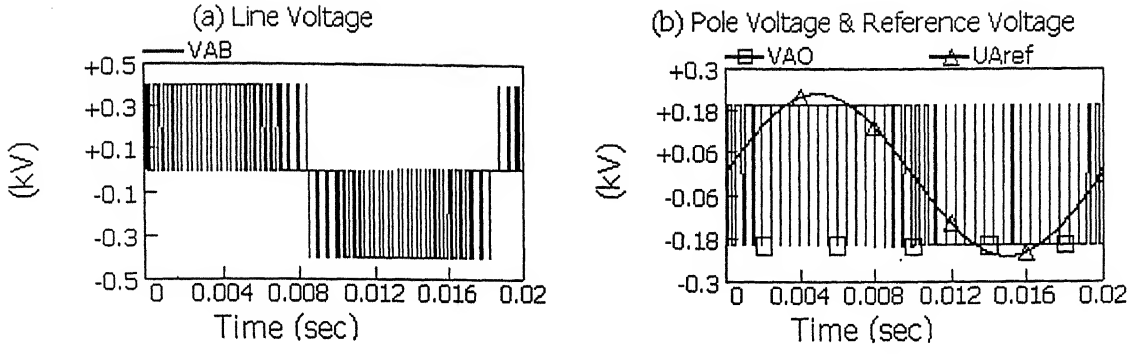


Fig. 2.5 (a) Line voltage and (b) Pole voltage and reference voltage for scheme 1 of switching sequence.

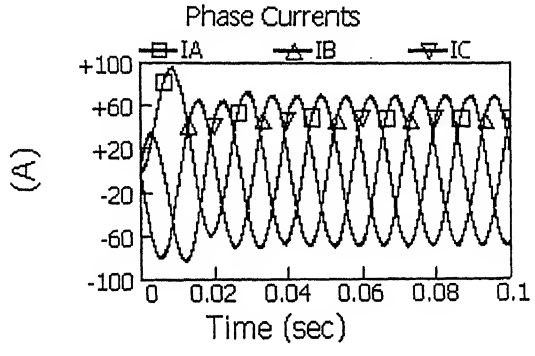


Fig. 2.6 Phase currents for scheme 1 of switching sequence.

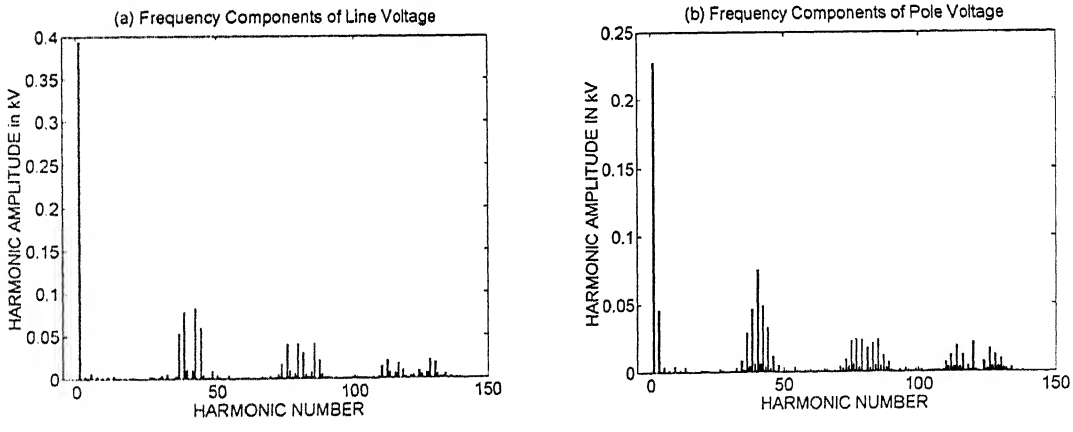


Fig. 2.7 Frequency components of (a) Line and (b) Pole voltage for scheme 1 of switching sequence.

Fig. 2.8, Fig. 2.9 and Fig. 2.10 shows the output results for scheme 2 of switching sequence and Fig. 2.11, Fig. 2.12 and Fig. 2.13 shows the output results for scheme 3.

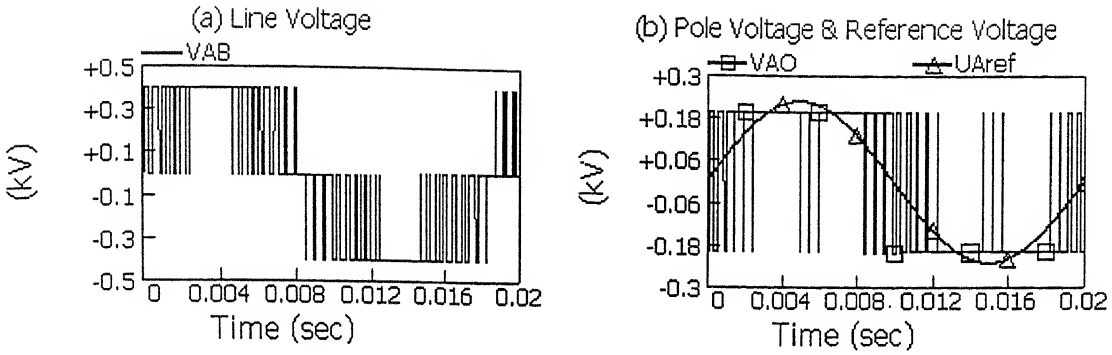


Fig. 2.8 (a) Line voltage and (b) Pole voltage and reference voltage for scheme 2 of switching sequence.

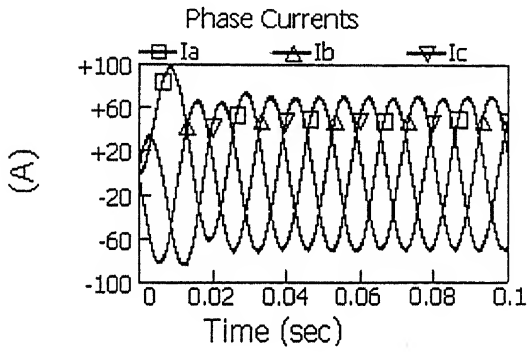


Fig. 2.9 Phase currents for scheme 2 of switching sequence.

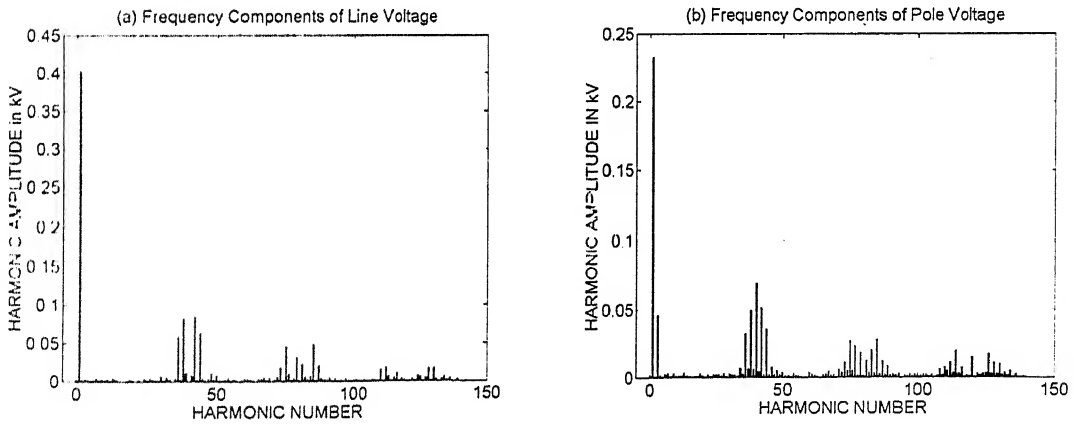


Fig. 2.10 Frequency components of (a) Line and (b) Pole voltage for scheme 2 of switching sequence.

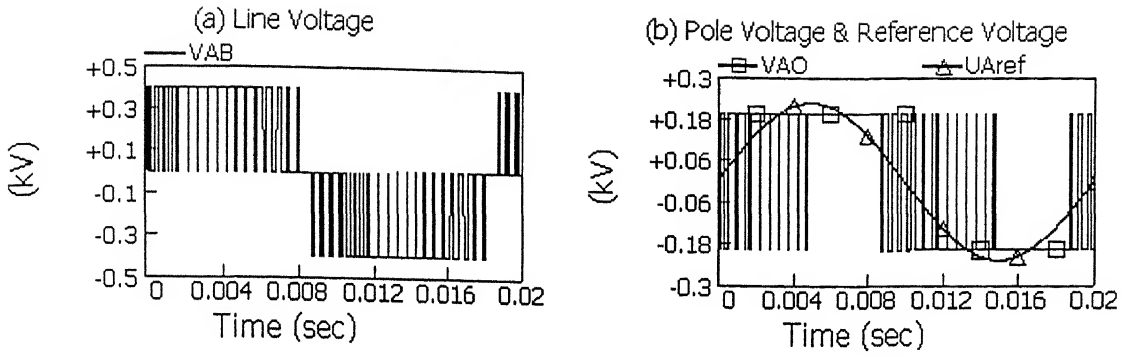


Fig. 2.11 (a) Line voltage and (b) Pole voltage and reference voltage for scheme 3 of switching sequence.

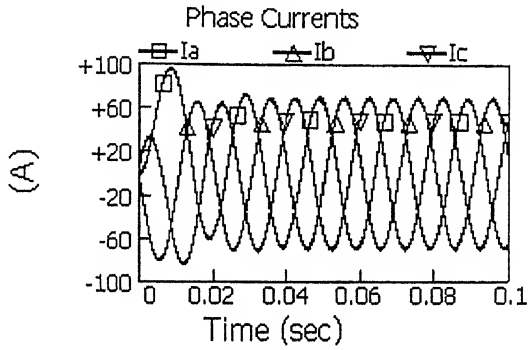


Fig. 2.12 Phase currents for scheme 3 of switching sequence.

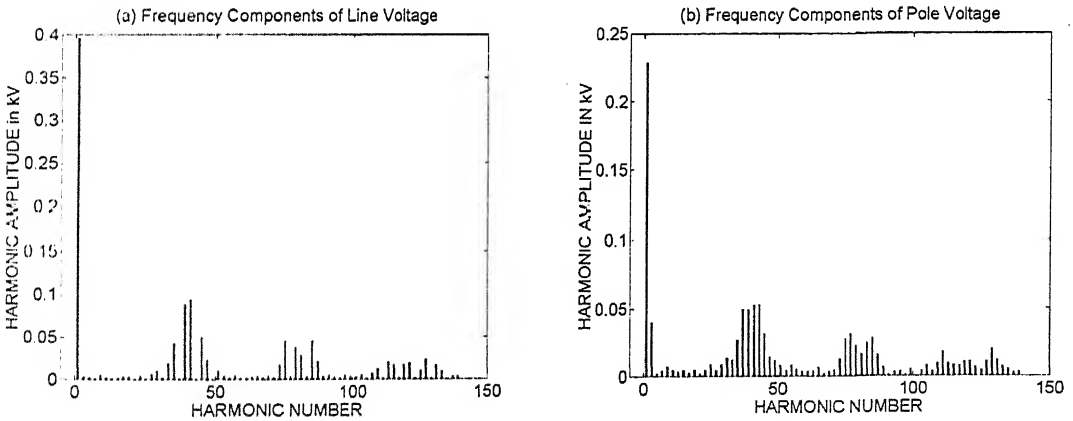


Fig. 2.13 Frequency components of (a) Line and (b) Pole voltage for scheme 3 of switching sequence.

2.2 SVM for Two-Level Four-Leg VSI

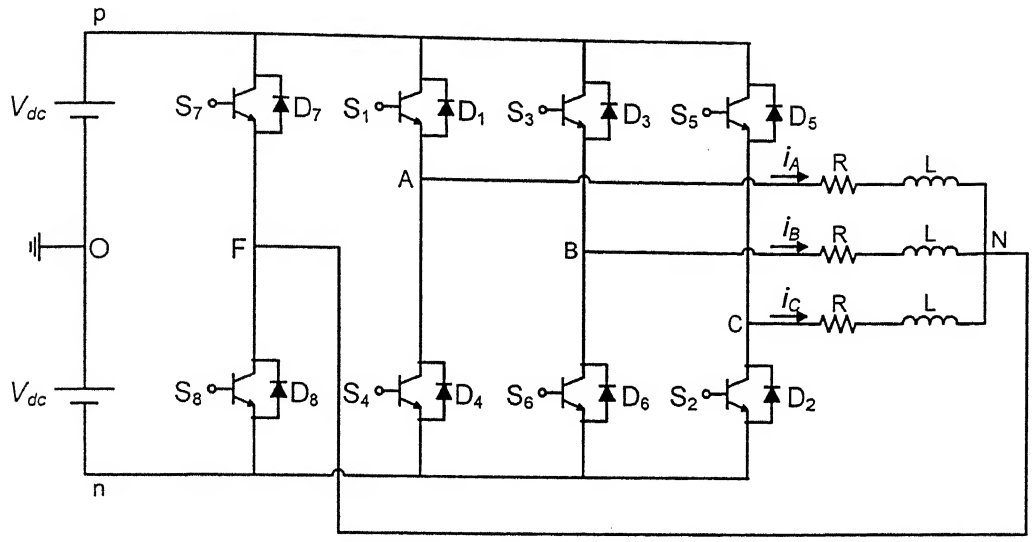


Fig 2.14 Two-level four-leg VSI with balanced RL load.

The four-leg VSI can be obtained by adding an additional leg (with switches S_8 and S_8 in series with anti-parallel diodes D_7 and D_8) to the three-leg VSI. The two-level four-leg VSI is shown in Fig. 2.14. It can be seen that the load neutral N is connected to the middle point of the fourth leg, F. This connection gives path for the zero sequence current to flow. As a result, this configuration will also work in the situations with voltage unbalance [12]. It is also useful for three-phase four-wire systems.

This inverter provides two levels of voltages $+V_{dc}$ and $-V_{dc}$ at the output terminals A, B and C with respect to the center point of dc source, O and three levels of voltages $+2V_{dc}$, 0 and $-2V_{dc}$ at the output terminals A, B and C with respect to the center point of the fourth leg, F.

2.2.1 Voltage Space Vectors in 3-Dimensional Space [13]

A traditional three-leg inverter has 8 possible switching combinations. With the additional fourth neutral leg the total number of switching combinations increases to 2^4=16. The switching combinations can be represented by the ordered sets $[m_F \quad m_A \quad m_B \quad m_C]$, where m_A='p' denotes that the upper switch in phase A, S_1 is closed and m_A='n' denotes

that the bottom switch in phase A, S_4 is closed. The same notation applies to phase legs B and C and to the fourth neutral leg.

Table 2.3 shows the resulting line-to-neutral voltages v_{AF}, v_{BF}, v_{CF} for all 16 switching combinations, i = $(m_F\ m_A\ m_B\ m_C)_2$. The ac terminal voltages $[v_{AF}\quad v_{BF}\quad v_{CF}]^T$ can be transformed into $[v_\alpha\quad v_\beta\quad v_\gamma]^T$ using

$$[v_\alpha\quad v_\beta\quad v_\gamma]^T = T\,[v_{AF}\quad v_{BF}\quad v_{CF}]^T \tag{2.27}$$

$$[v_{AF}\quad v_{BF}\quad v_{CF}]^T = T^{-1}\,[v_\alpha\quad v_\beta\quad v_\gamma]^T \tag{2.28}$$

where the transformation matrices T and T^1 are expressed as

$$T = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{2.29}$$

$$T^{-1} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \tag{2.30}$$

Let i, j, k be unit vectors in the α, β, γ space.

We define a switching vector in α, β, γ space as,

$$\overrightarrow{SV_i} = iv_\alpha + jv_\beta + kv_\gamma$$

where, v_α, v_β, v_γ are components defined by (2.27) for switching combination i=$(m_F$ $m_A\ m_B\ m_C)_2$ as listed in Table 2.3.

The results of the transformation are also shown in Table 2.3. They can be in turn plotted as 16 switching vectors in the 3-D space, as shown in Fig. 2.15. It should be noted that v_γ represents the zero-sequence component and is related to the neutral current. v_α and v_β are identical to the components of two dimensional vector defined earlier in (2.11).

TABLE 2.3

Phase voltages and voltage vectors for two-level four-leg VSI.

$[m_F\ m_A\ m_B\ m_C]$	v_{AF}	v_{BF}	v_{CF}	v_α	v_β	v_γ	Vector $\overline{SV_i}$
nnnn	0	0	0	0	0	0	$\overline{SV_0}$
nnnp	0	0	$2V_{dc}$	$-\frac{2}{3}V_{dc}$	$-\frac{2}{\sqrt{3}}V_{dc}$	$\frac{2}{3}V_{dc}$	$\overline{SV_1}$
nnpn	0	$2V_{dc}$	0	$-\frac{2}{3}V_{dc}$	$\frac{2}{\sqrt{3}}V_{dc}$	$\frac{2}{3}V_{dc}$	$\overline{SV_2}$
nnpp	0	$2V_{dc}$	$2V_{dc}$	$-\frac{4}{3}V_{dc}$	0	$\frac{4}{3}V_{dc}$	$\overline{SV_3}$
npnn	$2V_{dc}$	0	0	$\frac{4}{3}V_{dc}$	0	$\frac{2}{3}V_{dc}$	$\overline{SV_4}$
npnp	$2V_{dc}$	0	$2V_{dc}$	$\frac{2}{3}V_{dc}$	$-\frac{2}{\sqrt{3}}V_{dc}$	$\frac{4}{3}V_{dc}$	$\overline{SV_5}$
nppn	$2V_{dc}$	$2V_{dc}$	0	$\frac{2}{3}V_{dc}$	$\frac{2}{\sqrt{3}}V_{dc}$	$\frac{4}{3}V_{dc}$	$\overline{SV_6}$
nppp	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	0	0	$2V_{dc}$	$\overline{SV_7}$
pnnn	$-2V_{dc}$	$-2V_{dc}$	$-2V_{dc}$	0	0	$-2V_{dc}$	$\overline{SV_8}$
pnnp	$-2V_{dc}$	$-2V_{dc}$	0	$-\frac{2}{3}V_{dc}$	$-\frac{2}{\sqrt{3}}V_{dc}$	$-\frac{4}{3}V_{dc}$	$\overline{SV_9}$
pnpn	$-2V_{dc}$	0	$-2V_{dc}$	$-\frac{2}{3}V_{dc}$	$\frac{2}{\sqrt{3}}V_{dc}$	$-\frac{4}{3}V_{dc}$	$\overline{SV_{10}}$
pnpp	$-2V_{dc}$	0	0	$-\frac{4}{3}V_{dc}$	0	$-\frac{2}{3}V_{dc}$	$\overline{SV_{11}}$
ppnn	0	$-2V_{dc}$	$-2V_{dc}$	$\frac{4}{3}V_{dc}$	0	$-\frac{4}{3}V_{dc}$	$\overline{SV_{12}}$
ppnp	0	$-2V_{dc}$	0	$\frac{2}{3}V_{dc}$	$-\frac{2}{\sqrt{3}}V_{dc}$	$-\frac{2}{3}V_{dc}$	$\overline{SV_{13}}$
pppn	0	0	$-2V_{dc}$	$\frac{2}{3}V_{dc}$	$\frac{2}{\sqrt{3}}V_{dc}$	$-\frac{2}{3}V_{dc}$	$\overline{SV_{14}}$
pppp	0	0	0	0	0	0	$\overline{SV_{15}}$

The formation of the 16 switching vectors in 3-D α-β-γ space occurs when each of the eight switching vectors in the 2-D α-β plane for a two-level three-leg inverter combines with one of the two switching states of the neutral leg. There are two zero switching vectors and fourteen active switching vectors. These 16 vectors can be classified as follows according to their position in the 3-D space:

1. On layer $v_\gamma = 2V_{dc}$ sits the vector $\overline{SV_7}$.

2. On the layer $v_\gamma = \frac{4V_{dc}}{3}$ there are three active vectors: $\overline{SV_3}$, $\overline{SV_5}$ and $\overline{SV_6}$.

3. On the layer $v_\gamma = \frac{2V_{dc}}{3}$ there are three active vectors: $\overline{SV_1}$, $\overline{SV_2}$ and $\overline{SV_4}$.

4. The two zero vectors locate at the origin of the α-β-γ coordinate: $\overline{SV_0}$ and $\overline{SV_{15}}$.

5. On the layer $v_\gamma = -\frac{2V_{dc}}{3}$ there are three active vectors: $\overline{SV_{11}}$, $\overline{SV_{13}}$ and $\overline{SV_{14}}$.

6. On the layer $v_\gamma = -\frac{4V_{dc}}{3}$ there are three active vectors: $\overline{SV_9}$, $\overline{SV_{10}}$ and $\overline{SV_{12}}$.

7. On layer $v_\gamma = -2V_{dc}$ sits the vector $\overline{SV_{15}}$.

The index i of the vector $\overline{SV_i}$ corresponds to binary number $(m_F\ m_A\ m_B\ m_C)_2$.

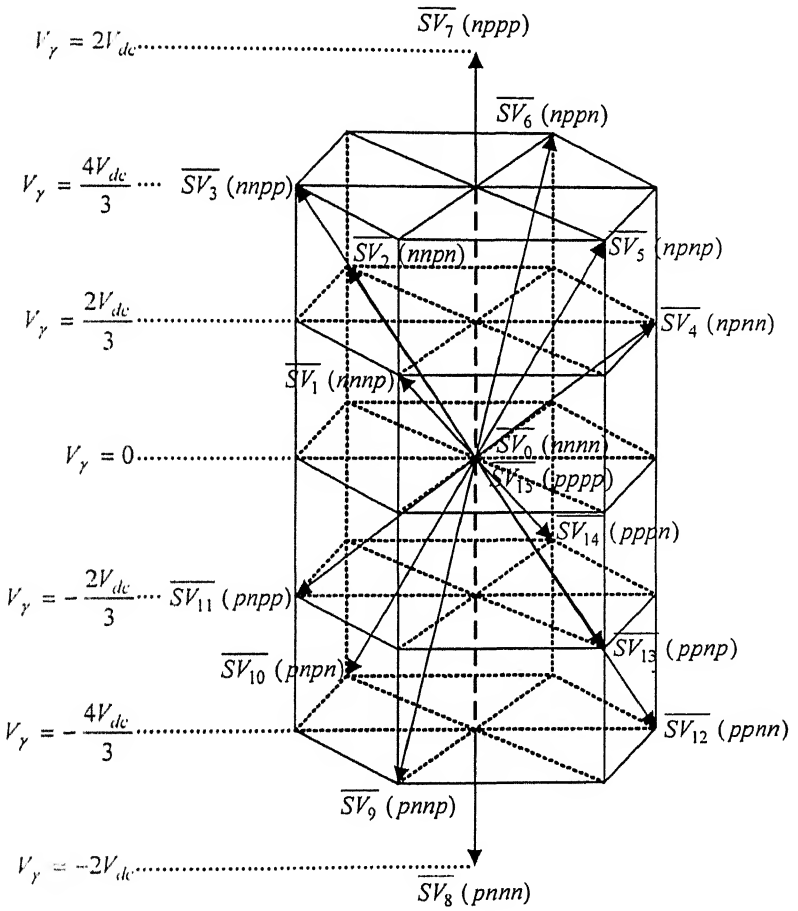


Fig. 2.15 Switching vectors $\overline{SV_i}$, i=$(m_F\ m_A\ m_B\ m_C)_2$, in 3-Dimension. $(m_F\ m_A\ m_B\ m_C)$ shown in bracket.

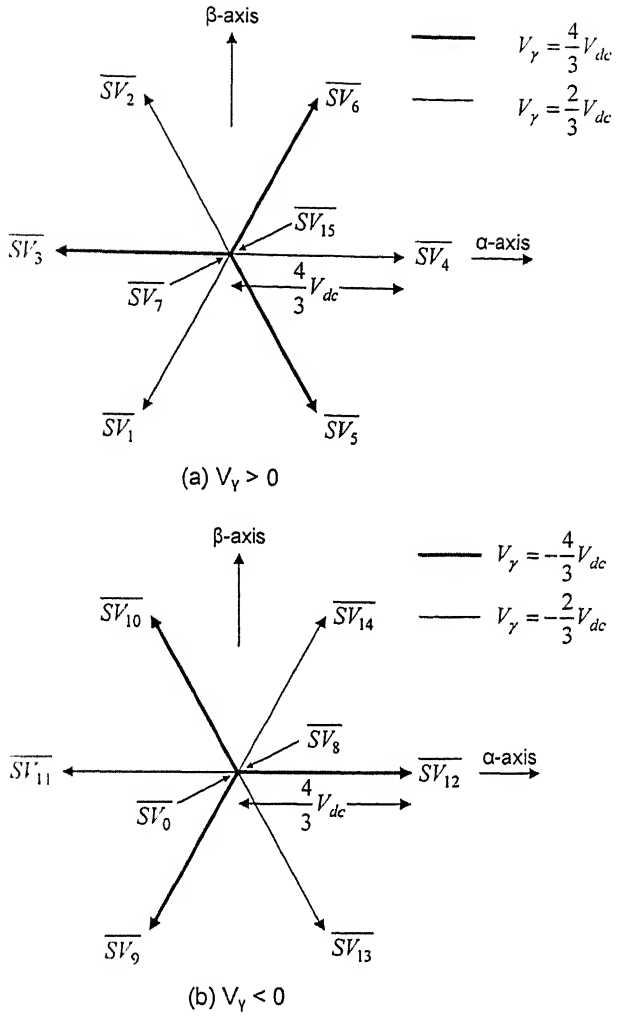


Fig. 2.16 Projection of the sixteen switching vectors back on the α-β plane.

Projection of the sixteen switching vectors back on the α-β plane forms a hexagon, which is the same as that of a conventional two-level three-leg converter. Therefore, 3-D space vectors are supersets of 2-D space vectors. The projected vectors have a length of $\frac{4V_{dc}}{3}$ on the plane. This is shown in Fig. 2.16.

2.2.2 Identification of the Nearest Voltage Space Vectors

Identification of the nearest vectors is straightforward for 2-D SVM, however, for 3-D SVM it takes two steps, namely prism identification and tetrahedron identification [13-15].

The vector space in 3-D can be divided into six prisms, identified and numbered as Prism 1 through 6, as shown in Fig. 2.17. Within the selected prism, there are six active vectors and two zero vectors, which divide the prism further into four tetrahedrons numbered as Tetrahedrons 1 through 24 for six prisms. As an example, the four tetrahedrons in Prism 1 are shown in Fig. 2.18.

2.2.2.1 Identification of Prism

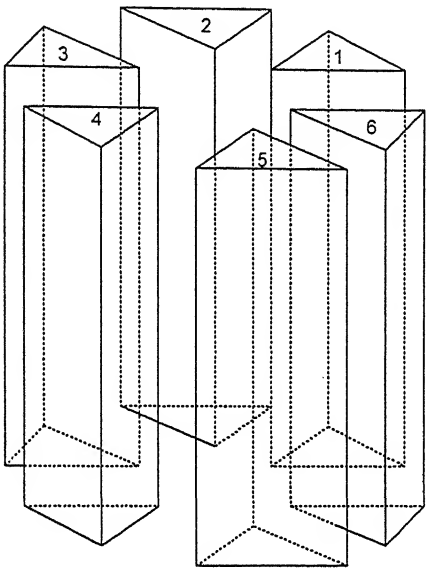


Fig. 2.17 Prism Identification.

The prism identification is very similar to the sector identification for 2-D SVM. As discussed earlier the projections of the switching vector on the α-β plane forms six active vectors and two zero vectors as shown in Fig. 2.16. Thus we have a hexagon having six sectors.

Now based on the projection of the reference vector on the α-β plane $v_{\alpha ref}$ and $v_{\beta ref}$, one of the six sectors can be selected in the same way as it was done for 2-D SVM in Section 2.1.3. Thus prism to be selected can be identified as the selected sector.

2.2.2.2 Identification of Tetrahedron

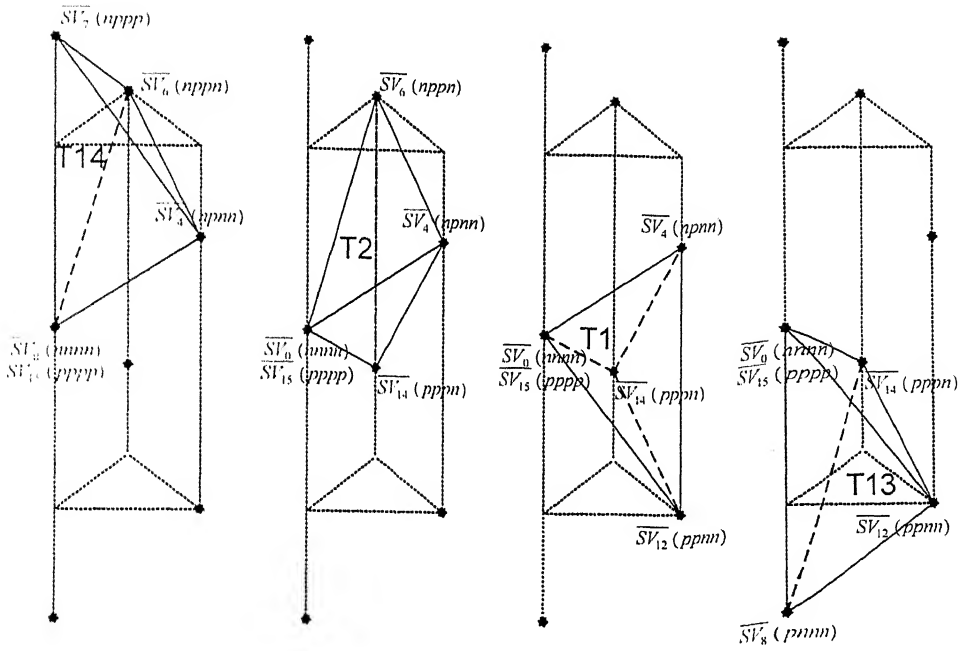


Fig. 2.18 Tetrahedron Identification.

Each tetrahedron has three active vectors and two zero vectors. The line-to-neutral voltage polarities produced by each active vector can be recognized as '+' or '–' or '0'. For example, the active vector $\overline{SV_4}$ (npnn) produces $[v_{AF} \quad v_{BF} \quad v_{CF}] = [+ \quad 0 \quad 0]$ line-to-neutral voltage polarities. It is important to notice that within each tetrahedron, all the active vectors produce unipolar line-to-neutral voltages, and thus they are nearest vectors. For example, three active vectors in Prism 1 and Tetrahedron 1 produce the ac terminal voltages $v_{AF} \geq 0, v_{BF} \leq 0$ *and* $v_{CF} \leq 0$.

The tetrahedron identification in the α-β-γ coordinate seems difficult since there is no simple mathematical expression available to tell in which tetrahedron the reference vector resides. A simple method to identify tetrahedron is based on the voltage polarities of the active vectors in the a-b-c coordinate. The voltage polarities of the reference vector in the a-b-c coordinate $[v_{AF\_ref} \quad v_{BF\_ref} \quad v_{CF\_ref}]$ are compared with those of the active vectors of each tetrahedron. The tetrahedron that encloses the reference vector has the active vectors with the same unipolar voltage polarities set. Table 2.4 shows the polarity

sets of reference voltages in a-b-c coordinate for tetrahedron identification. The exact values of line-to-neutral voltage v_{AF}, v_{BF}, v_{CF} for active vectors can be seen in Table 2.3.

TABLE 2.4

Tetrahedron Identification.

Prism	Tetrahedron	Vectors $\overline{SV_i}$ i = (m_F m_A m_B m_C)$_2$	Active Vectors	Polarity Set
P1	T1	4, 12, 14	npnn, ppnn, pppn	$v_{AF\ ref} \geq 0$, $v_{BF\ ref} < 0$, $v_{CF\ ref} < 0$
	T2	4, 6, 14	npnn, nppn, pppn	$v_{AF\ ref} \geq 0$, $v_{BF\ ref} \geq 0$, $v_{CF\ ref} < 0$
	T13	8, 12, 14	pnnn, ppnn, pppn	$v_{AF\ ref} < 0$, $v_{BF\ ref} < 0$, $v_{CF\ ref} < 0$
	T14	4, 6, 7	npnn, nppn, nppp	$v_{AF\ ref} \geq 0$, $v_{BF\ ref} \geq 0$, $v_{CF\ ref} \geq 0$
P2	T3	2, 6, 14	nnpn, nppn, pppn	$v_{AF\ ref} \geq 0$, $v_{BF\ ref} \geq 0$, $v_{CF\ ref} < 0$
	T4	2, 10, 14	nnpn, pnpn, pppn	$v_{AF\ ref} < 0$, $v_{BF\ ref} \geq 0$, $v_{CF\ ref} < 0$
	T15	8, 10, 14	pnnn, pnpn, pppn	$v_{AF\ ref} < 0$, $v_{BF\ ref} < 0$, $v_{CF\ ref} < 0$
	T16	2, 6, 7	nnpn, nppn, nppp	$v_{AF\ ref} \geq 0$, $v_{BF\ ref} \geq 0$, $v_{CF\ ref} \geq 0$
P3	T5	2, 10, 11	nnpn, pnpn, pnpp	$v_{AF\ ref} < 0$, $v_{BF\ ref} \geq 0$, $v_{CF\ ref} < 0$
	T6	2, 3, 11	nnpn, nnpp, pnpp	$v_{AF\ ref} < 0$, $v_{BF\ ref} \geq 0$, $v_{CF\ ref} \geq 0$
	T17	8, 10, 11	pnnn, pnpn, pnpp	$v_{AF\ ref} < 0$, $v_{BF\ ref} < 0$, $v_{CF\ ref} < 0$
	T18	2, 3, 7	nnpn, nnpp, nppp	$v_{AF\ ref} \geq 0$, $v_{BF\ ref} \geq 0$, $v_{CF\ ref} \geq 0$
P4	T7	1, 3, 11	nnnp, nnpp, pnpp	$v_{AF\ ref} < 0$, $v_{BF\ ref} \geq 0$, $v_{CF\ ref} \geq 0$
	T8	1, 9, 11	nnnp, pnnp, pnpp	$v_{AF\ ref} < 0$, $v_{BF\ ref} < 0$, $v_{CF\ ref} \geq 0$
	T19	8, 9, 11	pnnn, pnnp, pnpp	$v_{AF\ ref} < 0$, $v_{BF\ ref} < 0$, $v_{CF\ ref} < 0$
	T20	1, 3, 7	nnnp, nnpp, nppp	$v_{AF\ ref} \geq 0$, $v_{BF\ ref} \geq 0$, $v_{CF\ ref} \geq 0$
P5	T9	1, 9, 13	nnnp, pnnp, ppnp	$v_{AF\ ref} < 0$, $v_{BF\ ref} < 0$, $v_{CF\ ref} \geq 0$
	T10	1, 5, 13	nnnp, npnp, ppnp	$v_{AF\ ref} \geq 0$, $v_{BF\ ref} < 0$, $v_{CF\ ref} \geq 0$
	T21	8, 9, 13	pnnn, pnnp, ppnp	$v_{AF\ ref} < 0$, $v_{BF\ ref} < 0$, $v_{CF\ ref} < 0$
	T22	1, 5, 7	nnnp, npnp, nppp	$v_{AF\ ref} \geq 0$, $v_{BF\ ref} \geq 0$, $v_{CF\ ref} \geq 0$
P6	T11	4, 5, 13	npnn, npnp, ppnp	$v_{AF\ ref} \geq 0$, $v_{BF\ ref} < 0$, $v_{CF\ ref} \geq 0$
	T12	4, 12, 13	npnn, ppnn, ppnp	$v_{AF\ ref} \geq 0$, $v_{BF\ ref} < 0$, $v_{CF\ ref} < 0$
	T23	8, 12, 13	pnnn, ppnn, ppnp	$v_{AF\ ref} < 0$, $v_{BF\ ref} < 0$, $v_{CF\ ref} < 0$
	T24	4, 5, 7	npnn, npnp, nppp	$v_{AF\ ref} \geq 0$, $v_{BF\ ref} \geq 0$, $v_{CF\ ref} \geq 0$

2.2.3 Calculation of Switching Time

The time duration of the selected switching vectors can be easily computed by equating the reference vector to a weighted average of the active vectors. Assuming the reference vector $\overline{V_{ref}}$ is in Prism 1 and Tetrahedron 1, the available switching vectors are

$$\overline{V_1} = \overline{SV_4}$$

$$\overline{V_2} = \overline{SV_{12}}$$

$$\overline{V_3} = \overline{SV_{14}}$$

$$\overline{V_0} = [\overline{SV_0} \quad \overline{SV_{15}}]$$

The switching time for switching vectors can be calculated by,

$$\overline{V_{ref}} = \frac{T_1}{T_S}\overline{V_1} + \frac{T_2}{T_S}\overline{V_2} + \frac{T_3}{T_S}\overline{V_3} \tag{2.31}$$

Where T_1, T_2, T_3 are time durations for which the inverter remains in states corresponding to $\overline{V_1}, \overline{V_2}, \overline{V_3}$.

Equating the components in i, j, k directions, we get

$$\begin{bmatrix} V_{ref\_\alpha} \\ V_{ref\_\beta} \\ V_{ref\_\gamma} \end{bmatrix} = \frac{V_{dc}}{T_S} P \begin{bmatrix} T_1 \\ T_2 \\ T_3 \end{bmatrix} \tag{2.32}$$

where $P = \frac{1}{V_{dc}} \begin{bmatrix} V_{1\_\alpha} & V_{2\_\alpha} & V_{3\_\alpha} \\ V_{1\_\beta} & V_{2\_\beta} & V_{3\_\beta} \\ V_{1\_\gamma} & V_{2\_\gamma} & V_{3\_\gamma} \end{bmatrix}$ is the Projection Matrix. Inverting above equation, we get the required time durations,

$$\begin{bmatrix} T_1 \\ T_2 \\ T_3 \end{bmatrix} = \frac{T_S}{V_{dc}} P^{-1} \begin{bmatrix} V_{ref\_\alpha} \\ V_{ref\_\beta} \\ V_{ref\_\gamma} \end{bmatrix} \tag{2.33}$$

$$T_Z = T_S - T_1 - T_2 - T_3 \tag{2.34}$$

For the reference vector in other tetrahedrons equations similar to (2.33) can be written with the corresponding projection matrix P. The complete table for the corresponding active vectors and matrices to compute the switching time for all 24 tetrahedrons is given in Appendix A.

2.2.4 Switching Sequence for 3-D SVM

Similar to their 2-D SVM counterpart, the sequencing schemes for 3-D SVM can be classified in three schemes. In 3-D SVM there are three active vectors in each half-carrier period compared to two for 2-D SVM. Here the switching sequence for Tetrahedron 1 of Prism 1 of the 3-D space vector phasor space is given. A similar sequence is readily

established for the other tetrahedrons. Fig. 2.19 shows the pulse pattern for Tetrahedron 1 of Prism 1 for all the three schemes.

2.2.4.1 Scheme 1: Active Space Vector Pulses Centered at the Middle of the Sampling Period

The conventional SVM implementation with active space vector pulses centered in the middle of each half-carrier period and the remaining time split equally between $\overline{SV_0}$ and $\overline{SV_{15}}$ creates a space vector sequence (for Tetrahedron 1 of Prism 1) of:

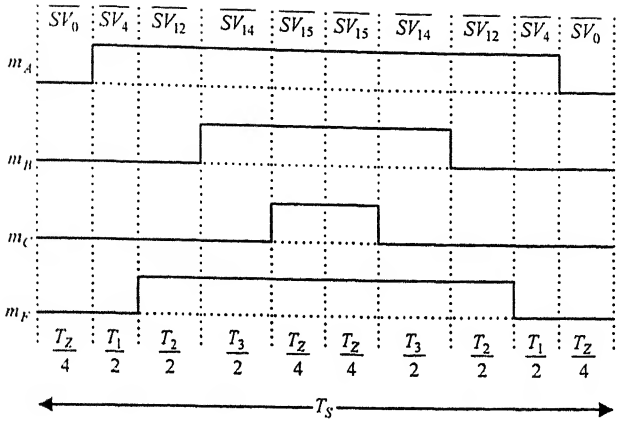
$$\underbrace{\overline{SV_0} \rightarrow \overline{SV_4} \rightarrow \overline{SV_{12}} \rightarrow \overline{SV_{14}} \rightarrow \overline{SV_{15}}}_{\frac{T_S}{2}} \rightarrow \underbrace{\overline{SV_{15}} \rightarrow \overline{SV_{14}} \rightarrow \overline{SV_{12}} \rightarrow \overline{SV_4} \rightarrow \overline{SV_0}}_{\frac{T_S}{2}} \tag{2.35}$$

It should be noted from (2.35) that there are three active vectors in each half-carrier period and their sequence reverses over a complete carrier interval. Further, the zero space vectors $\overline{SV_0}$ and $\overline{SV_{15}}$ are placed in such a way that transition from one state to another makes only one switch to change its state. The sequence of (2.35) can be implemented with the active space vector periods T_1, T_2 *and* T_3 recalculated every half-carrier period or once per entire T_S.

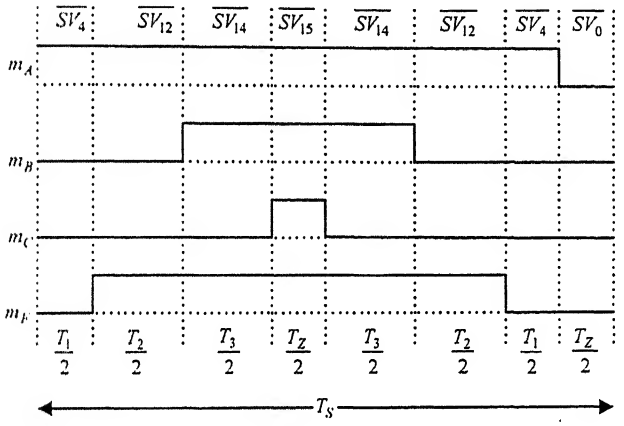
2.2.4.2 Scheme 2: High Quality SVM Pulses

In this scheme only one of the two zero vectors is used in each half-carrier period. The two zero vectors $\overline{SV_0}$ and $\overline{SV_{15}}$ are placed at the end of each alternate half-carrier period. Particular zero vector for each half-carrier period is chosen such that transition from one state to another makes only one switch to change its state. For the same purpose, sequence of active space vectors is reversed over a complete carrier period. The resulting space vector sequence for Tetrahedron 1 of Prism 1 is:

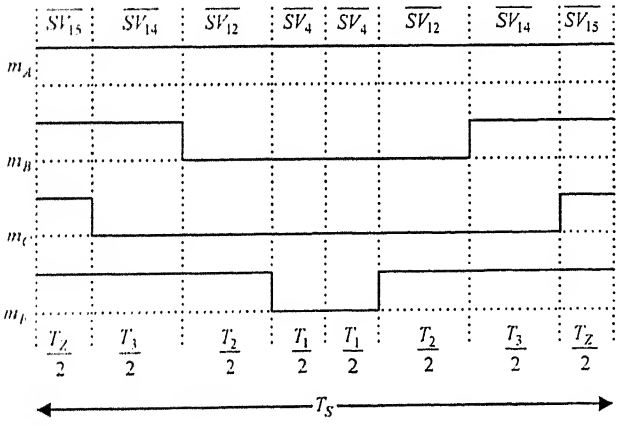
$$\underbrace{\overline{SV_4} \rightarrow \overline{SV_{12}} \rightarrow \overline{SV_{14}} \rightarrow \overline{SV_{15}}}_{\frac{T_S}{2}} \rightarrow \underbrace{\overline{SV_{14}} \rightarrow \overline{SV_{12}} \rightarrow \overline{SV_4} \rightarrow \overline{SV_0}}_{\frac{T_S}{2}} \tag{2.36}$$



(a)



(b)



(c)

Fig. 2.19 Pulse pattern of space vector modulation for Tetrahedron 1 of Prism 1 with (a) centered active space vectors, (b) high quality pulses, (c) high efficiency pulses.

2.2.4.3 Scheme 3: High Efficiency SVM Pulses

In this scheme only one of the two zero vectors is used in each carrier period. One of the two zero space vectors $\overline{SV_Z} = [\overline{SV_0} \quad \overline{SV_{15}}]$ is placed at the start and at the end of each alternating half-carrier period. So, there are two kinds of sequences: one with $\overline{SV_0}$ and the other with $\overline{SV_{15}}$. The active vector sequences are chosen such that transition from one state to another makes only one switch to change its state. The resulting space vector sequence for Tetrahedron 1 of Prism 1 is (with $\overline{SV_0}$):

$$\begin{array}{c} \overline{SV_0} \rightarrow \overline{SV_4} \rightarrow \overline{SV_{12}} \rightarrow \overline{SV_{14}} \rightarrow \overline{SV_{14}} \rightarrow \overline{SV_{12}} \rightarrow \overline{SV_4} \rightarrow \overline{SV_0} \\ \left|\longleftarrow \frac{T_S}{2} \longrightarrow\right\|\left\|\longleftarrow \frac{T_S}{2} \longrightarrow\right| \end{array} \tag{2.37}$$

The resulting space vector sequence for Tetrahedron 1 of Prism 1 is (with $\overline{SV_{15}}$):

$$\begin{array}{c} \overline{SV_{15}} \rightarrow \overline{SV_{14}} \rightarrow \overline{SV_{12}} \rightarrow \overline{SV_4} \rightarrow \overline{SV_4} \rightarrow \overline{SV_{12}} \rightarrow \overline{SV_{14}} \rightarrow \overline{SV_{15}} \\ \left|\longleftarrow \frac{T_S}{2} \longrightarrow\right\|\left\|\longleftarrow \frac{T_S}{2} \longrightarrow\right| \end{array} \tag{2.38}$$

2.2.5 Simulation Results

System parameters chosen for simulation of two-level four-leg VSI with balanced RL load as shown in Fig. 2.14 are given in Table 2.2. The output line-line voltage, pole voltage and reference voltage are shown in Fig. 2.20 for scheme 1 of switching sequence. Fig. 2.21 shows the phase currents and Fig. 2.22 shows frequency components of line and phase voltages. It should be noted here that the phase voltage and line voltage does not contain third harmonic component but pole voltage contains third harmonic component.

Fig. 2.23, Fig. 2.24 and Fig. 2.25 shows the output results for scheme 2 of switching sequence and Fig. 2.26, Fig. 2.27 and Fig. 2.28 shows the output results for scheme 3.

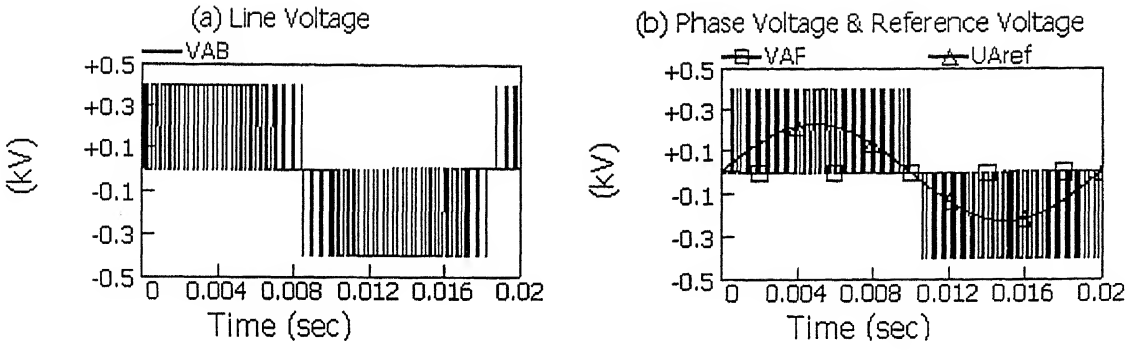


Fig. 2.20 (a) Line voltage and (b) Phase voltage and reference voltage for scheme 1 of switching sequence.

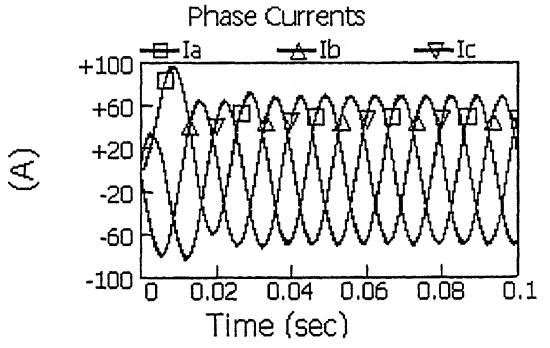


Fig. 2.21 Phase currents for scheme 1 of switching sequence.

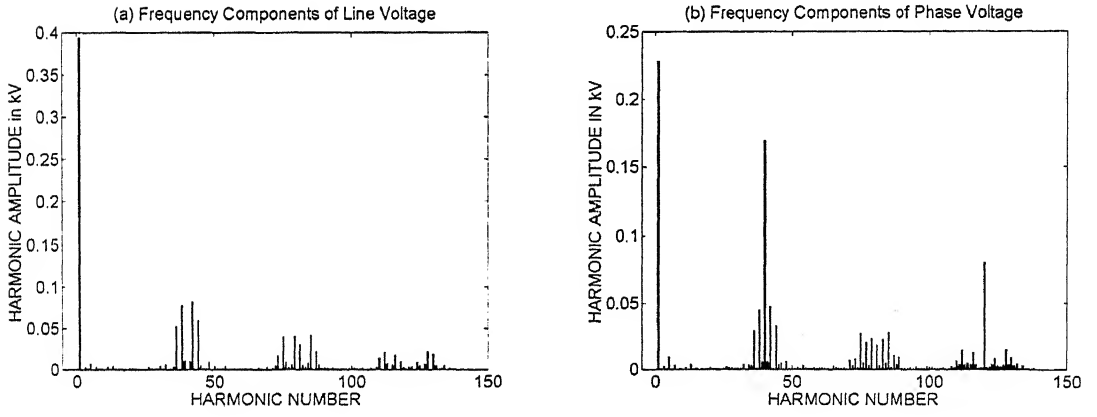


Fig. 2.22 Frequency components of (a) Line and (b) Phase voltage for scheme 1 of switching sequence.

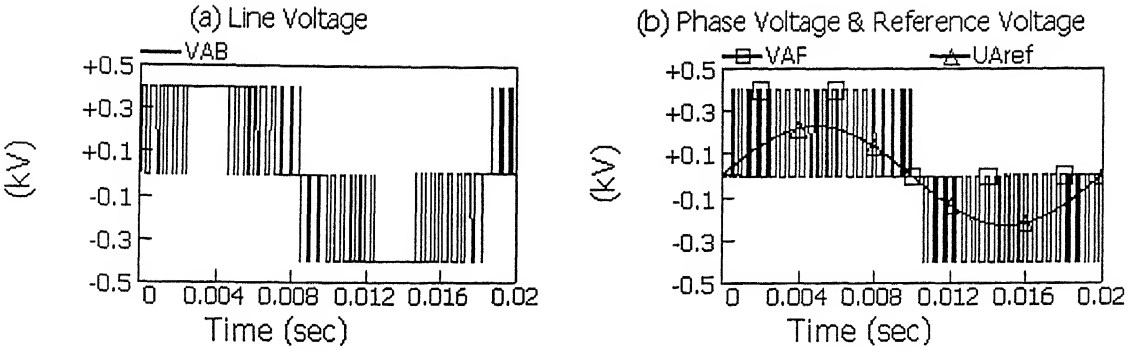


Fig. 2.23 (a) Line voltage and (b) Phase voltage and reference voltage for scheme 2 of switching sequence.

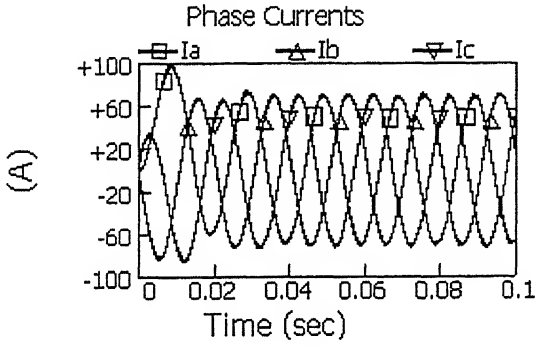


Fig. 2.24 Phase currents for scheme 2 of switching sequence.

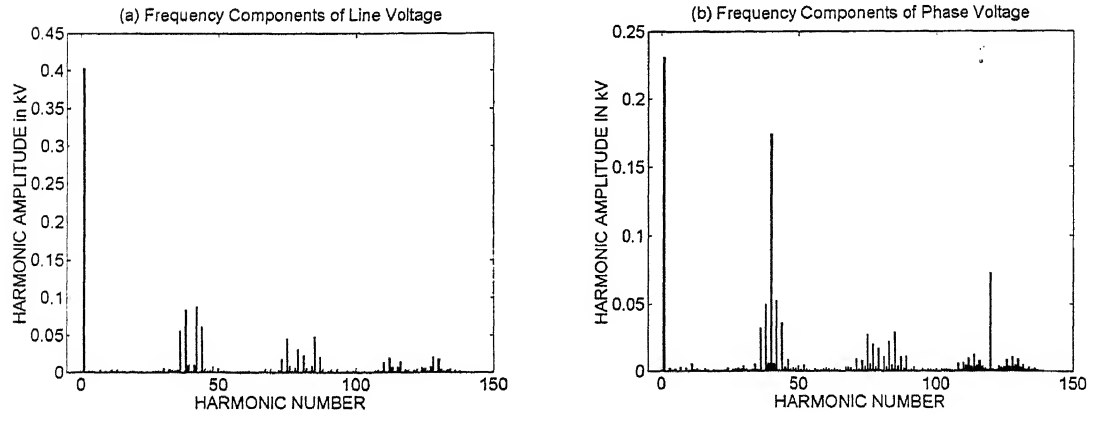


Fig. 2.25 Frequency components of (a) Line and (b) Phase voltage for scheme 2 of switching sequence.

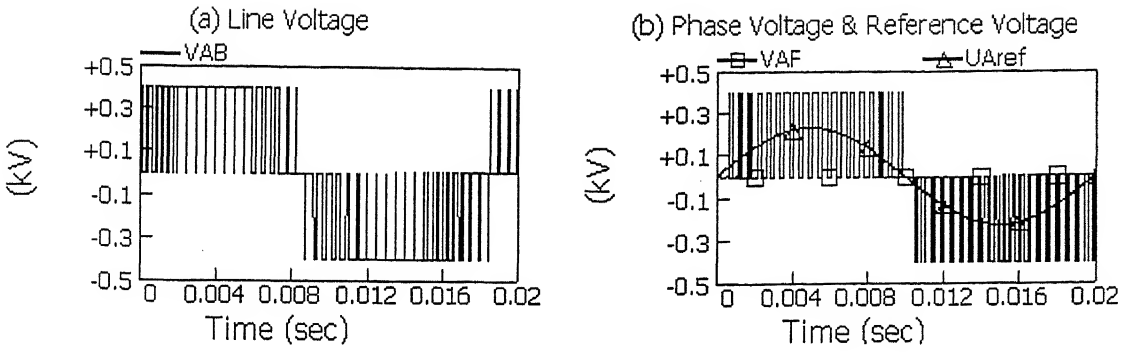


Fig. 2.26 (a) Line voltage and (b) Phase voltage and reference voltage for scheme 3 of switching sequence.

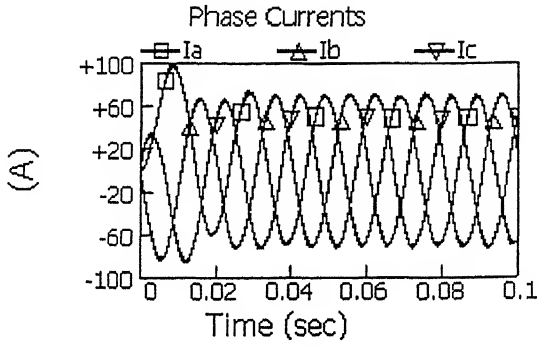


Fig. 2.27 Phase currents for scheme 3 of switching sequence.

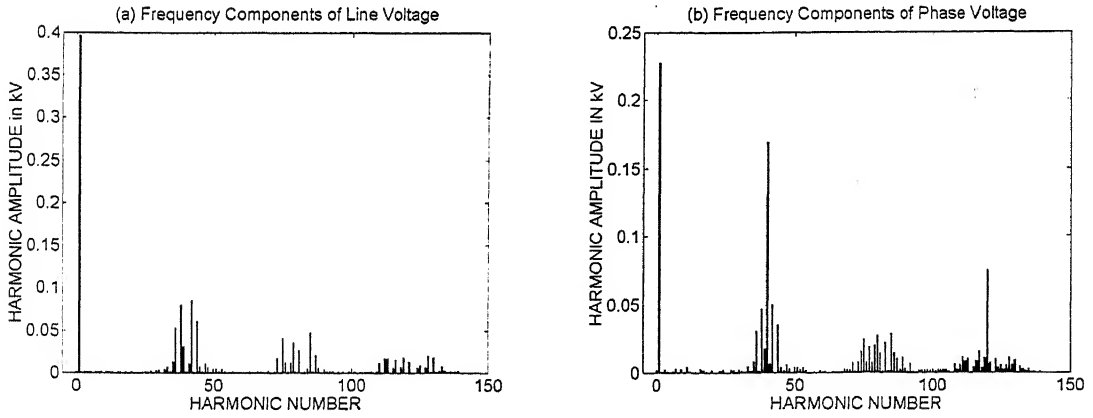


Fig. 2.28 Frequency components of (a) Line and (b) Phase voltages for scheme 3 of switching sequence.

Simulation for 2-level 4-leg VSI of Fig. 2.14 is repeated for unbalanced load and system parameters chosen for the simulation are given in Table 2.5. Fig. 2.29 and Fig. 2.30 shows the output results for this case.

TABLE 2.5

System Parameters for two-level four-leg VSI with unbalanced RL load.

System Parameters	Values of Parameters
dc Voltage	$2V_{dc} = 400$ Volts
Load Resistor	$R_A = 1.0\ \Omega$, $R_B = 2.0\ \Omega$, $R_C = 3.0\ \Omega$
Load Inductor	$L_A = 0.01$ H, $L_B = 0.02$ H, $L_C = 0.03$ H
Sampling Frequency	$F_S = 2000$ Hz

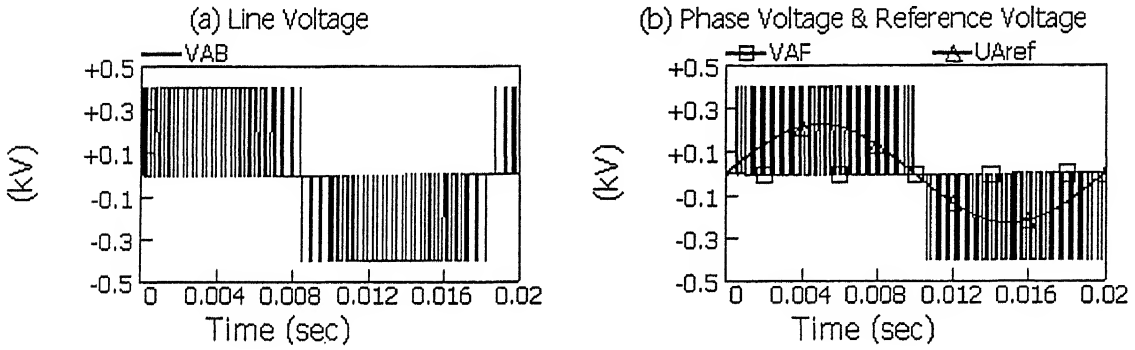


Fig. 2.29 (a) Line voltage and (b) Phase voltage and reference voltage for two-level four-leg VSI with unbalanced RL load for scheme 1 of switching sequence.

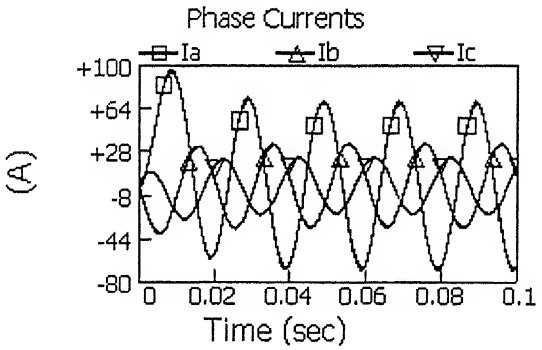


Fig. 2.30 Phase Currents for two-level four-leg VSI with unbalanced RL load with scheme 1 of switching sequence.

2.3 SVM for Three-Level Diode Clamped VSI

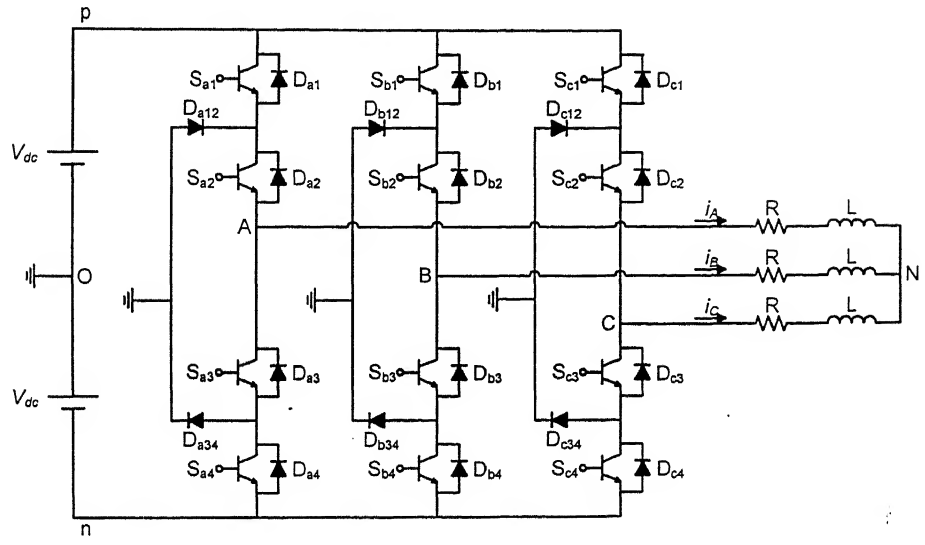


Fig. 2.31 Three-level diode clamped VSI with balanced RL load.

A three-level diode clamped VSI is shown in Fig. 2.31. It consists of 12 switches with anti-parallel diodes. There are four switches (S_{x1}...S_{x4}, x=a, b, c) in each of the three legs. The dc source is divided into two parts with ground as the center point, O. The junctions of the upper two switches and lower two switches in each leg is connected through diodes to the center point, O. E.g., junction of S_{a1} and S_{a2} is connected through D_{a12}. There are six such diodes. Use of these diodes facilitates current flow in both directions. The three-phase output is provided at points A, B and C. As compared to two-level invert, which provides two levels of output $+V_{dc}$ and $-V_{dc}$, this inverter provides three levels of voltages $+V_{dc}$, 0 and $-V_{dc}$ at the output terminals A, B and C with respect to the center point of dc source, O.

The major benefit of this configuration is that, while there are twice as many switches as in the two-level inverter, each of the switches must block only one-half of the dc link voltage (as is the case for the six center-tapped diodes). Which means high power levels can be attained. Another advantage is reduced harmonic content in the output voltage [16].

2.3.1 Voltage Space Vectors for Three-Level Inverter

The inverter provides output voltages of V_{dc}, 0 and $-V_{dc}$, by closing a combination of two switches in each leg. For phase A, point 'A' can be connected to +ve terminal 'p' of dc source by closing S_{a1} and S_{a2}, to O by closing S_{a2} and S_{a3}, and to –ve terminal 'n' of dc source by closing S_{a3} and S_{a4}. The same is true for the other two phases also. The use of diodes ensures that the output voltage level is independent of the direction of output current.

The analysis of Section 2.1.1 for two-level three-leg VSI and (2.1) to (2.12) are valid for three-level three-leg VSI also. The only difference is that the switching states m_A, m_B and m_C can now have three values instead of two. The output of each of the three states can be defined as '1', '0' or '-1' according to the switching state of the 12 switches, as shown in Table 2.6.

TABLE 2.6

The inverter switching states.

$m_A = 1$	$v_{AO} = V_{dc}$	S_{a1} and S_{a2} are ON
$m_A = 0$	$v_{AO} = 0$	S_{a2} and S_{a3} are ON
$m_A = -1$	$v_{AO} = -V_{dc}$	S_{a3} and S_{a4} are ON
$m_B = 1$	$v_{BO} = V_{dc}$	S_{b1} and S_{b2} are ON
$m_B = 0$	$v_{BO} = 0$	S_{b2} and S_{b3} are ON
$m_B = -1$	$v_{BO} = -V_{dc}$	S_{b3} and S_{b4} are ON
$m_C = 1$	$v_{AO} = V_{dc}$	S_{c1} and S_{c2} are ON
$m_C = 0$	$v_{AO} = 0$	S_{c2} and S_{c3} are ON
$m_C = -1$	$v_{AO} = -V_{dc}$	S_{c3} and S_{c4} are ON

As switching states m_A, m_B and m_C are independent and as there are only three possible values for each switching state, there are $3^3 = 27$ switching combinations. So we have 27 possible values for pole voltages and phase voltages as shown in Table 2.7. A particular phase voltage, e.g. v_{AN}, can attain only nine different values of output voltage. Of these four are +ve, four are –ve and one is zero, as compared to 2-level inverter that can attain a total of five values of voltages.

The pole voltage vector can be defined as in (2.11) and is written again here as

$$\overline{V} = \frac{2}{3}\left(V_{AN} + aV_{BN} + a^2 V_{CN}\right) \tag{2.39}$$

where $a = e^{j\frac{2\pi}{3}}$.

TABLE 2.7

Pole voltages, phase voltages and voltage vectors for three-level VSI.

m_A	m_B	m_C	v_{AO}	v_{BO}	v_{CO}	v_{AN}	v_{BN}	v_{CN}	$\|V\|$	$\angle V$	Voltage Vector
−1	−1	−1	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$	0	0	0	0	0°	$\overline{SV_{24}}$
−1	−1	0	$-V_{dc}$	$-V_{dc}$	0	$-\frac{V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	−120°	$\overline{SV_4}$
−1	−1	1	$-V_{dc}$	$-V_{dc}$	V_{dc}	$-\frac{2V_{dc}}{3}$	$-\frac{2V_{dc}}{3}$	$\frac{4V_{dc}}{3}$	$\frac{4V_{dc}}{3}$	−120°	$\overline{SV_{22}}$
−1	0	−1	$-V_{dc}$	0	$-V_{dc}$	$-\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	120°	$\overline{SV_2}$
−1	0	0	$-V_{dc}$	0	0	$-\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	180°	$\overline{SV_3}$
−1	0	1	$-V_{dc}$	0	V_{dc}	$-V_{dc}$	0	V_{dc}	$\frac{2V_{dc}}{\sqrt{3}}$	−150°	$\overline{SV_{15}}$
−1	1	−1	$-V_{dc}$	V_{dc}	$-V_{dc}$	$-\frac{2V_{dc}}{3}$	$\frac{4V_{dc}}{3}$	$-\frac{2V_{dc}}{3}$	$\frac{4V_{dc}}{3}$	120°	$\overline{SV_{20}}$
−1	1	0	$-V_{dc}$	V_{dc}	0	$-V_{dc}$	V_{dc}	0	$\frac{2V_{dc}}{\sqrt{3}}$	150°	$\overline{SV_{14}}$
−1	1	1	$-V_{dc}$	V_{dc}	V_{dc}	$-\frac{4V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$\frac{4V_{dc}}{3}$	180°	$\overline{SV_{21}}$
0	−1	−1	0	$-V_{dc}$	$-V_{dc}$	$\frac{2V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	0°	$\overline{SV_0}$
0	−1	0	0	$-V_{dc}$	0	$\frac{V_{dc}}{3}$	$-\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	−60°	$\overline{SV_5}$
0	−1	1	0	$-V_{dc}$	V_{dc}	0	$-V_{dc}$	V_{dc}	$\frac{2V_{dc}}{\sqrt{3}}$	−90°	$\overline{SV_{16}}$
0	0	−1	0	0	$-V_{dc}$	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$-\frac{2V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	60°	$\overline{SV_1}$
0	0	0	0	0	0	0	0	0	0	0°	$\overline{SV_{25}}$
0	0	1	0	0	V_{dc}	$-\frac{V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	−120°	$\overline{SV_{10}}$
0	1	−1	0	V_{dc}	$-V_{dc}$	0	V_{dc}	$-V_{dc}$	$\frac{2V_{dc}}{\sqrt{3}}$	90°	$\overline{SV_{13}}$
0	1	0	0	V_{dc}	0	$-\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	120°	$\overline{SV_8}$
0	1	1	0	V_{dc}	V_{dc}	$-\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	180°	$\overline{SV_9}$
1	−1	−1	V_{dc}	$-V_{dc}$	$-V_{dc}$	$\frac{4V_{dc}}{3}$	$-\frac{2V_{dc}}{3}$	$-\frac{2V_{dc}}{3}$	$\frac{4V_{dc}}{3}$	0°	$\overline{SV_{18}}$
1	−1	0	V_{dc}	$-V_{dc}$	0	V_{dc}	$-V_{dc}$	0	$\frac{2V_{dc}}{\sqrt{3}}$	−30°	$\overline{SV_{17}}$
1	−1	1	V_{dc}	$-V_{dc}$	V_{dc}	$\frac{2V_{dc}}{3}$	$-\frac{4V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$\frac{4V_{dc}}{3}$	−60°	$\overline{SV_{23}}$
1	0	−1	V_{dc}	0	$-V_{dc}$	V_{dc}	0	$-V_{dc}$	$\frac{2V_{dc}}{\sqrt{3}}$	30°	$\overline{SV_{12}}$
1	0	0	V_{dc}	0	0	$\frac{2V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	0°	$\overline{SV_6}$
1	0	1	V_{dc}	0	V_{dc}	$\frac{V_{dc}}{3}$	$-\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	−60°	$\overline{SV_{11}}$
1	1	−1	V_{dc}	V_{dc}	$-V_{dc}$	$\frac{2V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$-\frac{4V_{dc}}{3}$	$\frac{4V_{dc}}{3}$	60°	$\overline{SV_{19}}$
1	1	0	V_{dc}	V_{dc}	0	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$-\frac{2V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	60°	$\overline{SV_7}$
1	1	1	V_{dc}	V_{dc}	V_{dc}	0	0	0	0	0°	$\overline{SV_{26}}$

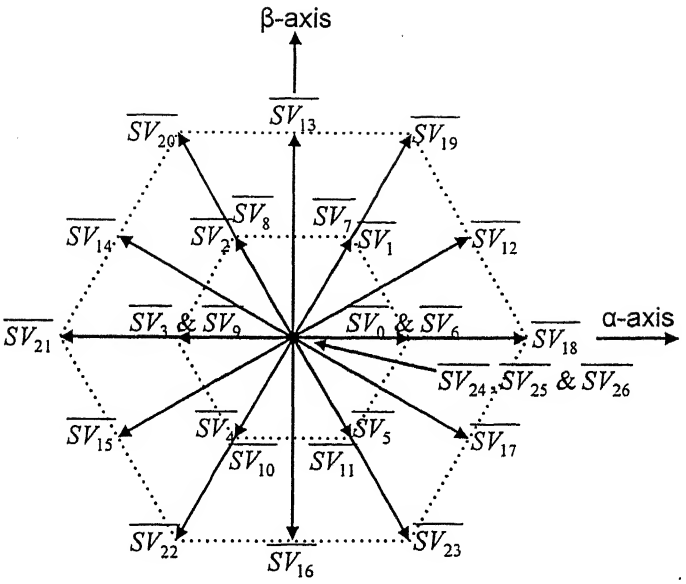


Fig. 2.32 Twenty-Seven possible stationary vectors in complex plane for a three-level VSI.

The 27 voltage values give voltage vectors distributed at different angles in the complex plane. The voltage vectors in the complex plane are shown in Fig. 2.32. These can be grouped as follows:

1. Large Vectors $\overline{SV_L}$: Six vectors ($\overline{SV_{18}}$ to $\overline{SV_{23}}$) of magnitude $\frac{4}{3}V_{dc}$ are distributed in space with 60° phase difference from each other.
2. Medium Vectors $\overline{SV_M}$: Six vectors ($\overline{SV_{12}}$ to $\overline{SV_{17}}$) of magnitude $\frac{2}{\sqrt{3}}V_{dc}$ distributed in space with 60° phase difference from each other and the entire group shifted by 30° from the group of vectors of large vectors.
3. Small Vectors $\overline{SV_S}$: Twelve vectors ($\overline{SV_0}$ to $\overline{SV_{11}}$) of magnitude $\frac{2}{3}V_{dc}$ in six pairs of coincident vectors of two each, distributed in space with phase difference of 60° from each other.
4. Zero Vectors $\overline{SV_Z}$: There are three vectors ($\overline{SV_{24}}$ to $\overline{SV_{26}}$) with zero magnitude located at the origin of the plane.

2.3.2 Space Vector Modulation Scheme I

In this SVM technique, the 2-D α-β plane is divided into twelve sectors as shown in Fig. 2.32, separated by different voltage space vectors. Once the reference vector has been found, the next step is to find the sector in which this reference vector lies. Depending on the value of θ_{ref} one of the twelve sectors can be selected.

In each sector there are 4 active vectors: one large vector, one medium vector and two small vectors. We can use any two of these four vectors to generate the reference voltage vector along with the three zero vectors.

2.3.2.1 Identification of the Voltage Space Vectors and Calculation of Switching Time

It is found that there are four active vectors for each sector. At any point in time, an arbitrary target output voltage vector $\overline{V_{ref}}$ can be formed by summation of a number of these space vectors within one switching period T_S. The selection of the space vectors depends on the magnitude and angle of required voltage vector, $\overline{V_{ref}}$, as explained below.

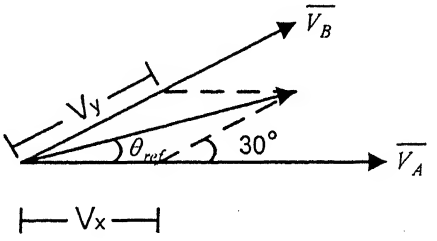


Fig. 2.33 Components of voltage vector $\overline{V_{ref}}$ in the direction $\overline{V_A}$ and $\overline{V_B}$.

The angle θ_{ref} and the two inverter voltage vectors $\overline{V_A}$ and $\overline{V_B}$, between which the voltage vector $\overline{V_{ref}}$ lies, are found, as shown in Fig.2.33. One of them is a medium vector and the other is a large vector The conduction times T_A for vector $\overline{V_A}$, T_B for vector $\overline{V_B}$ and T_C for zero vector is calculated, that would approximate total vector, on an average during the carrier period, T_S.

$$\overline{V_{ref}} = \frac{T_A \overline{V_A} + T_B \overline{V_B}}{T_S} \tag{2.40}$$

Let $\overline{V_x}$ and $\overline{V_y}$ be the components of $\overline{V_{ref}}$ in the direction of vector $\overline{V_A}$ and $\overline{V_B}$ respectively, as shown in Fig. 2.33, therefore

$$\overline{V_{ref}} = \overline{V_x} + \overline{V_y} \tag{2.41}$$

Magnitudes of $\overline{V_x}$ and $\overline{V_y}$ can be calculated as,

$$V_y = 2V_{ref} \sin\theta_{ref} \tag{2.42}$$

$$V_x = V_{ref} \cos\theta_{ref} - \frac{\sqrt{3}}{2} V_y \tag{2.43}$$

Thus from (2.40) and (2.41)

$$T_A = \frac{V_x}{V_A} T_S \tag{2.44}$$

$$T_B = \frac{V_y}{V_B} T_S \tag{2.45}$$

$$T_Z = T_S - T_A - T_B \tag{2.46}$$

The above result can be directly applied to approximate $\overline{V_{ref}}$ by space vectors in Fig. 2.33. However there are multiple vectors in the same direction, e.g. $\overline{SV_0}$, $\overline{SV_6}$ and $\overline{SV_{18}}$. The selection of appropriate vector can be done by following criteria.

1. The time T_A+T_B should be less than or equal to the carrier period T_S.
2. The switching of devices in the inverter should be minimum.

For example, let the reference vector lies in between $\overline{SV_{18}}$ and $\overline{SV_{12}}$ as shown in Fig. 2.34. There are two more vectors, $\overline{SV_0}$ and $\overline{SV_6}$ in the direction of $\overline{SV_{18}}$ but only one of these is to be selected.

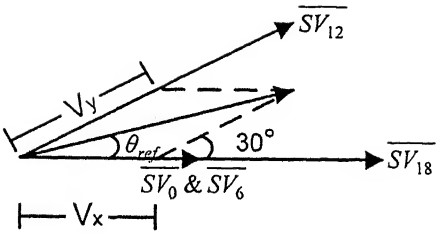


Fig. 2.34 Components of voltage vector $\overline{V_{ref}}$ in the direction $\overline{SV_{18}}$ and $\overline{SV_{12}}$.

$\overline{V_x}$ and $\overline{V_y}$ are the components of vector $\overline{V_{ref}}$ in the direction of $\overline{SV_{18}}$ and $\overline{SV_{12}}$ respectively. Their magnitudes are calculated from (2.42) and (2.43). T_A, T_B and T_C are calculated as

$$T_A = \frac{V_x}{\left|\overline{SV_0}\right|} T_S \tag{2.47}$$

$$T_B = \frac{V_y}{\left|\overline{SV_{12}}\right|} T_S \tag{2.48}$$

$$T_Z = T_S - T_A - T_B \tag{2.49}$$

If $T_A+T_B<T_S$, $\overline{SV_0}$ or $\overline{SV_6}$ is to be selected.

If $T_A+T_B>T_S$, $\overline{SV_{18}}$ is selected, T_B remains the same but T_A is recalculated as

$$T_A = \frac{V_x}{\left|\overline{SV_{18}}\right|} T_S \tag{2.50}$$

$$T_Z = T_S - T_A - T_B \tag{2.51}$$

$\overline{SV_0}$ and $\overline{SV_6}$ are equal vectors, so the state corresponding to any of them can be selected. The choice depends upon the minimum switching required to move to the vector $\overline{SV_{12}}$.

Here T_Z is the time for zero space vectors. Balance of the carrier period is made up of any combination of the zero space vectors $\overline{SV_{24}}$, $\overline{SV_{25}}$ and $\overline{SV_{26}}$. This freedom of choice allows the placement of the space vectors to be varied anywhere within the carrier period to obtain required harmonic or switching performance.

2.3.2.2 Switching Sequence

For each 30° sector, proper small or large vector is to be selected to generate required reference voltage vector. Once this selection is done, we get following switching sequences.

- Sequence when the selected vector is a small vector.
- Sequence when the selected vector is a large vector.

Here the switching sequence for the first 30° sector of the space vector phasor space with active space vectors centered in the middle of the half-carrier period is described. A similar sequence is readily established for other sectors using the nearest space vector components for each sector.

When small vector is selected we get the following sequence. For example, $\overline{SV_S} = \overline{SV_0}$ *or* $\overline{SV_6}$ and $\overline{SV_M} = \overline{SV_{12}}$ for $0 \le \theta_{ref} \le \frac{\pi}{6}$.

$$\begin{aligned} &\overline{SV_Z} \rightarrow \overline{SV_S} \rightarrow \overline{SV_M} \rightarrow \overline{SV_M} \rightarrow \overline{SV_S} \rightarrow \overline{SV_Z} \\ &|\longleftarrow\!\!\!\!\!\!- T_S -\!\!\!\!\!\!\longrightarrow|\longleftarrow\!\!\!\!\!\!- T_S -\!\!\!\!\!\!\longrightarrow| \end{aligned} \tag{2.52}$$

When large vector is selected we get the following sequence. For example, $\overline{SV_L} = \overline{SV_{18}}$ and $\overline{SV_M} = \overline{SV_{12}}$ for $0 \le \theta_{ref} \le \frac{\pi}{6}$.

$$\begin{aligned} &\overline{SV_Z} \rightarrow \overline{SV_L} \rightarrow \overline{SV_M} \rightarrow \overline{SV_M} \rightarrow \overline{SV_L} \rightarrow \overline{SV_Z} \\ &|\longleftarrow\!\!\!\!\!\!- T_S -\!\!\!\!\!\!\longrightarrow|\longleftarrow\!\!\!\!\!\!- T_S -\!\!\!\!\!\!\longrightarrow| \end{aligned} \tag{2.53}$$

(2.52) and (2.53) shows the switching sequence when switching time is calculated for each carrier period. Fig. 2.35 shows the pulse pattern in the first 30° sector for conventional space vector PWM with equally spaced zero space vectors for both of the above cases.

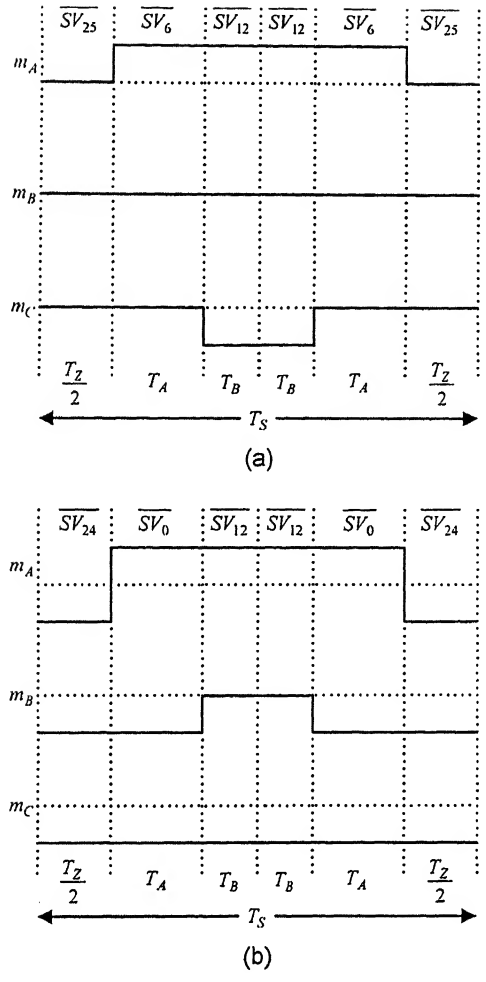


Fig. 2.35 Pulse patterns of space vector modulation scheme 1 in the first sector, $0 \le \theta_{ref} \le \frac{\pi}{6}$ with centered active space vectors.

2.3.3 Space Vector Modulation Scheme II [10]

The 27 possible voltage vectors of the three-level VSI, can be visualized to be contained in a hexagon as shown in Fig. 2.32. The large and middle vectors fall on the boundary of this 'outer' hexagon. The twelve small vectors lie on an 'inner' hexagon. Since there are 27 possible states, the complexity of selecting the proper states for a given reference voltage vector can be considerably simplified by viewing the three-level inverter space vector hexagon as consisting of six two level hexagons, as shown in Fig. 2.36 [17]. A 'two level' hexagon is similar to that of a 2 level SVM. The origin of each of these six 'two level' hexagons, is located on one of the apexes of 'inner' hexagon of the three level

inverter. Thus each of the two-level hexagons is shifted by $2V_{dc}/3$, in six different directions, with respect to the origin of the three-level hexagons, both inner and outer. In Fig. 2.36 the 'two level' hexagons are shown. Three in dotted lines and three in solid lines. Their centers are number 1 to 6.

To proceed with the switching state determination, there are two steps to be followed. First, one of the six hexagons is selected based on the location of the target voltage vector. Second, the vector that locates the origin of the selected two-level hexagon is subtracted from the original reference vector to obtain a new reference vector for the two level hexagon.

After these two steps, determination of the switching sequence and the calculation of the voltage vector duration can be done in the same manner as for a conventional two-level inverter. For this purpose the new (reduced) reference vector is used.

2.3.3.1 Identifying Two-Level Hexagon

The choice of the two-level hexagon should be such that the reference voltage vector smoothly progresses from one hexagon to the next as it rotates. Subdividing the vector space into six regions as shown in Fig. 2.37 and selecting the two-level hexagon from Fig. 2.36 whose center number corresponds to the region number, satisfies this requirement.

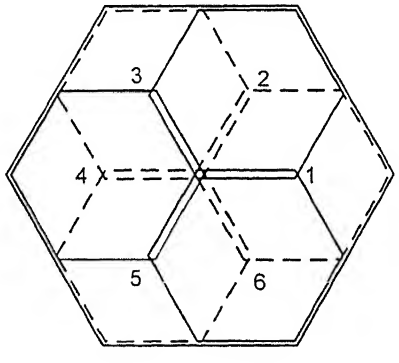


Fig. 2.36 Space vector hexagon of a three-level inverter viewed as being composed of six two-level hexagons.

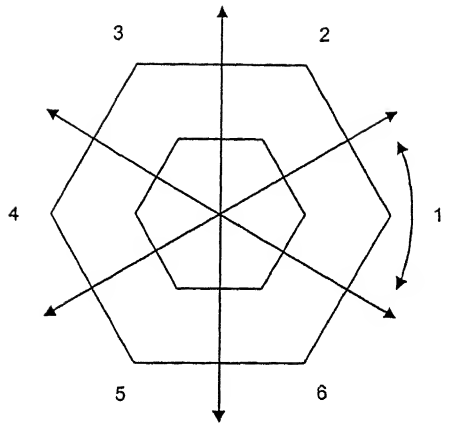


Fig. 2.37 Segregation of three-level hexagon into six sectors s = 1, 2...6.

2.3.3.2 Change of Reference Voltage Vector

Once the sector is identified, the origin of the reference voltage vector is changed to the origin of the two-level hexagon associated with that sector. This is achieved by subtracting a vector locating the center of the selected hexagon from the original reference vector.

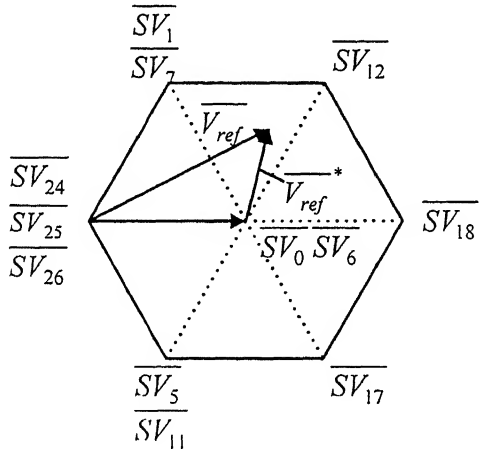


Fig. 2.38 Example showing change of reference origin for a reference voltage vector $\overline{V_{ref}}$ located in Sector 1.

For example, let the reference vector $\overline{V_{ref}}$ be in sector 1. So, hexagon 1 is selected. Then vector locating the center of the hexagon 1 is subtracted from the reference vector

$\overline{V_{ref}}$ to give new reference vector $\overline{V_{ref}}^{*}$ with reference origin at the center of the hexagon 1 as shown in Fig. 2.38.

2.3.3.3 Switching Sequence

In this SVM technique the three-level hexagon is identified to be composed of six two-level hexagons. One of these six hexagons is selected based on the location of the reference voltage vector and then the original reference voltage vector is decremented by the voltage vector that locates the origin of the selected two-level hexagon. After this procedure, we can apply the same switching sequence schemes of two-level SVM technique as discussed in Section 2.1.5.

2.3.4 Simulation Results

System parameters chosen for simulation of three-level three-leg VSI with balanced RL load are given in Table 2.8. The output line-line voltage, phase voltage and reference voltage are shown in Fig. 2.39 for SVM scheme 1 with active pulses centered at the middle of the half-carrier period. Fig. 2.40 shows the phase currents and Fig. 2.41 shows the frequency components of line and pole voltages.

TABLE 2.8

System Parameters for two-level three-leg VSI with balanced RL load.

System Parameters	Values of Parameters
dc Voltage	$2V_{dc} = 400$ Volts
Load Resistor	$R = 1.0\ \Omega$
Load Inductor	$L = 0.01$ H
Sampling Frequency	$F_S = 1800$ Hz

Fig. 2.42, Fig. 2.43 and Fig. 2.44 shows the output results for SVM scheme 2.

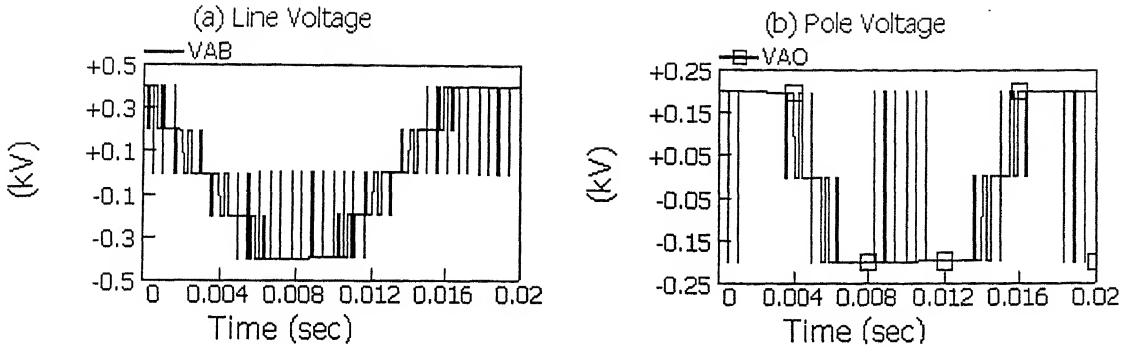


Fig. 2.39 (a) Line voltage and (b) Pole voltage for SVM scheme1.

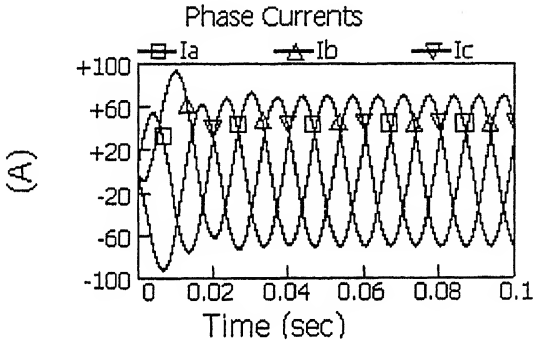


Fig. 2.40 Phase currents for SVM scheme 1.

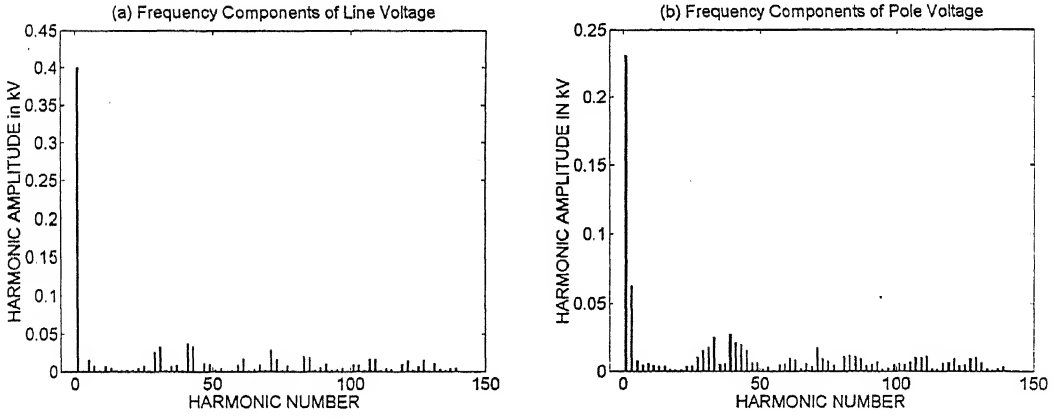


Fig. 2.41 Frequency components of (a) Line and (b) Pole voltages for SVM scheme 1.

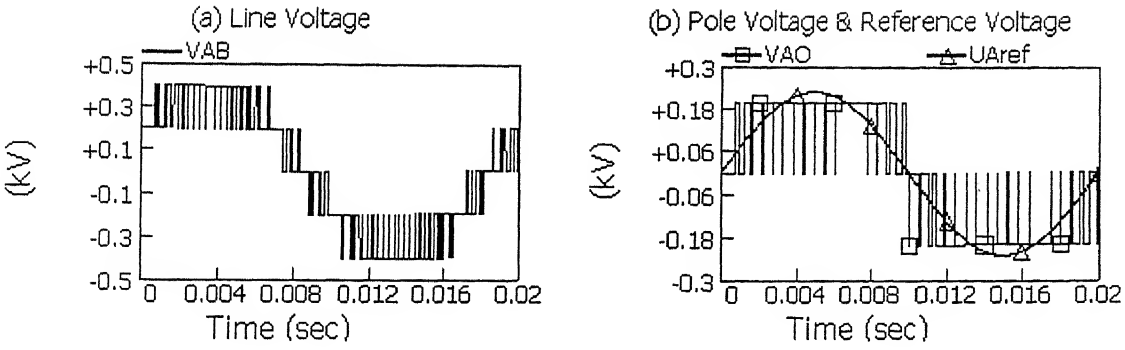


Fig. 2.42 (a) Line voltage and (b) Pole voltage for SVM scheme 2.

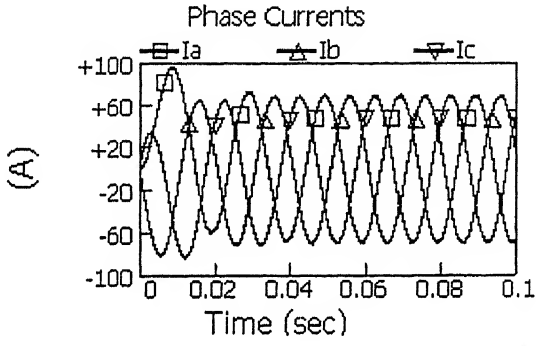


Fig. 2.43 Phase currents for SVM scheme 2.

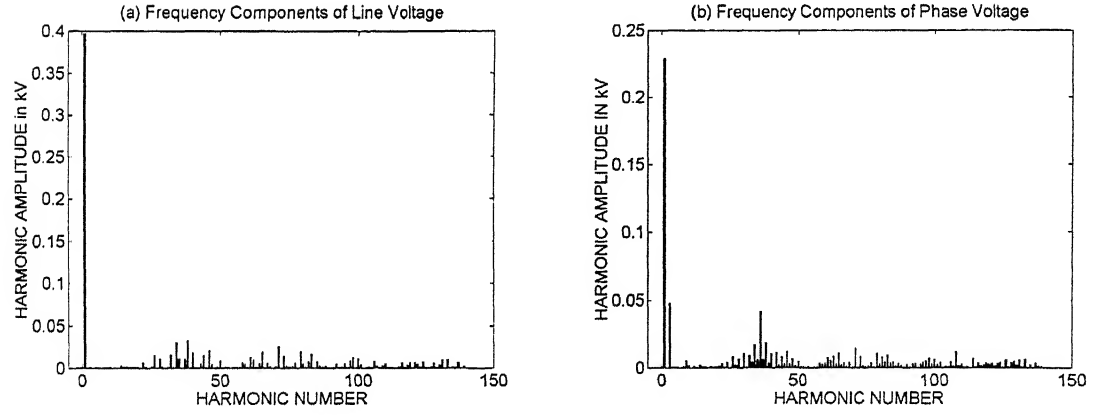


Fig. 2.44 Frequency components of (a) Line and (b) Pole voltages for SVM scheme 2.

2.4 Comparison of Harmonic Performance

Table 2.9 gives the Total Harmonic Distortion (THD) in pole and line-to-line voltage for two-level three-leg VSI and three-level diode clamped VSI and also phase and line-to-line voltage for two-level four-leg VSI. The amplitude modulation index used is 1.15 and the dc source voltage is 400 V for all the schemes.

It can be seen that the THD of the pole voltages is much higher compared to that of the line-to-line voltages for two-level three-leg VSI and three-level diode clamped VSI. This is mainly due to the presence of third harmonic component in the pole voltages. The THD in the phase voltages of the two-level four-leg VSI is less because the phase voltages does not contain third harmonic component.

If the THD in the line-to-line voltages are compared, then it can be seen that the line-to-line voltage of SVM scheme 2 for three-level diode clamped VSI is minimum.

TABLE 2.9

THD in pole, phase and line-to-line voltages for various schemes of SVM used for different VSI configurations.

	THD in pole voltage (%)	THD in line-line voltage (%)
	2-D SVM for two-level three-leg VSI	
Scheme 1	20.19	2.188
Scheme 2	17.63	1.189
Scheme 3	19.78	1.51
	2-D SVM for three-level diode clamped VSI	
SVM Scheme 1	27.57	4.419
SVM Scheme 2	21.04	0.4723
	3-D SVM for three-level diode clamped VSI	
	THD in phase voltage (%)	THD in line-line voltage (%)
Scheme 1	4.56	2.188
Scheme 2	2.32	0.9197
Scheme 3	2.27	1.543

CHAPTER 3

DYNAMIC VOLTAGE RESTORER OPERATION USING SPACE VECTOR MODULATION

A power electronic converter based series compensator that can protect critical loads from all supply side disturbances other than outages is called a dynamic voltage restorer (DVR). It is basically a series compensator. A series compensator protects a sensitive load from the distortion in the supply side voltage. The basic principle of a series compensator is simple: by inserting a voltage of required magnitude and frequency, the series compensator can restore the load side voltage to the desired amplitude and waveform even when the source voltage is unbalanced or distorted [18-19].

3.1 Dynamic Voltage Restorer

The DVR is made of a solid-state dc to ac switching power converter (inverter) that injects a set of three-phase ac output voltages in series and synchronism with the distribution feeder voltages. The dc input terminal of the DVR is connected to an energy source or an energy storage device of appropriate capacity. The reactive power exchanged between the DVR and the distribution system is internally generated by the DVR without ac passive reactive components. The real power exchanged at the DVR output ac terminals is provided by the DVR input dc terminal by an external energy source or energy storage system [20].

A typical DVR connection is shown in Fig. 3.1. It is connected in series with the distribution feeder-2 that supplies a sensitive load. For a fault clearing or switching at point A of the incoming feeder or fault in the distribution feeder-1, the voltage at feeder-2 will sag. Without the presence of the DVR, this will trip the sensitive load causing a loss of production. The DVR can protect the sensitive load by inserting voltages of controllable amplitude, phase angle and frequency (fundamental and harmonic) into the distribution

feeder via a series insertion transformer shown in Fig. 3.1. It is however to be mentioned that the rating of a DVR is not unlimited. Thus a DVR can only supply partial power to the load during very large variations (sags or swells) in the source voltage.

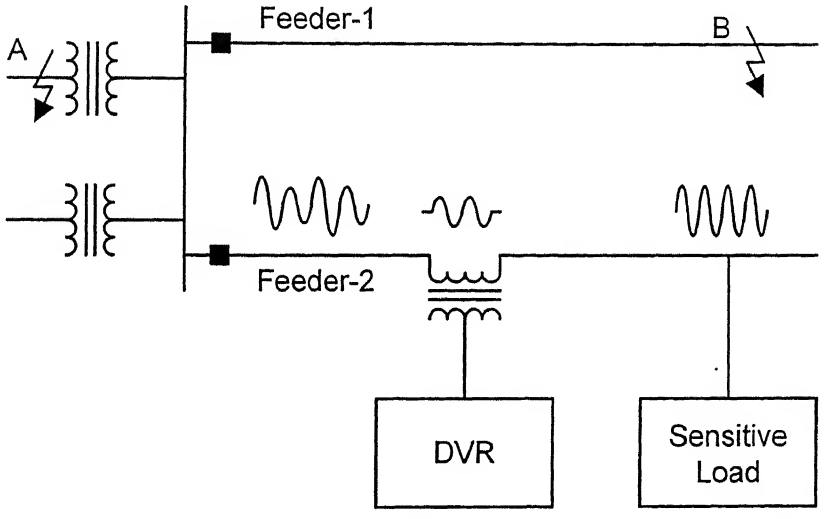


Fig. 3.1 DVR connection for voltage sag correction for sensitive loads.

Two DVR dc bus supply strategies will be discussed here. They are

1. DVR supplied by a dc battery.
2. DVR supplied from the feeder through a rectifier.

Both of these configurations are shown in Fig. 3.2.

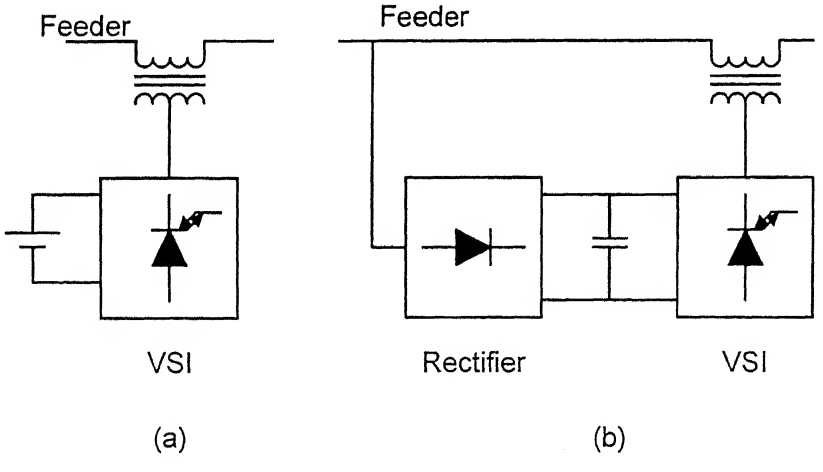


Fig. 3.2 Two possible dc bus supply strategies of DVR (a) supported by dc battery, (b) supported by rectifier.

3.2 DVR Structure

The DVR is made of a solid-state dc to ac switching power converter (inverter) that is usually a voltage source inverter (VSI). The VSI is connected to the network through three single-phase transformers. The transformers not only reduce the voltage requirement of the inverters but also provide isolation between the VSI and the higher voltage ac system. The dc to ac converters generate PWM output voltages that contain harmonics. Unfortunately these voltage harmonics give rise to current harmonics, which propagate through the feeder. Therefore filters are needed to provide a path for the harmonic currents to flow.

The filtering scheme in a DVR can be placed either on the high-voltage side or on the low-voltage inverter side of the series injection transformer. A filtering scheme in which the filter is placed on the high-voltage side is shown in Fig. 3.3, while Fig. 3.4 shows the low-voltage side filtering scheme.

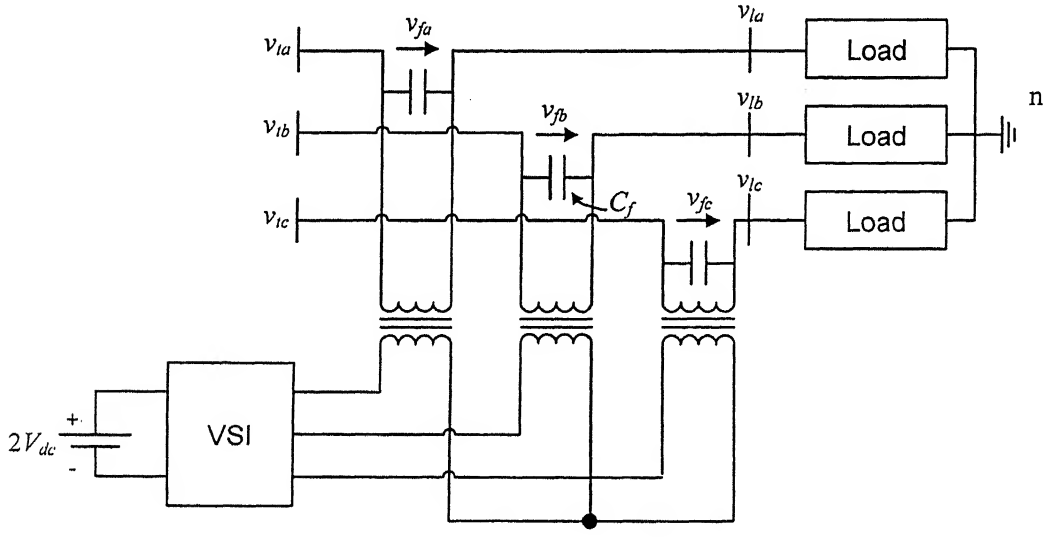


Fig. 3.3 DVR structure with capacitor filter.

In the filter structure of Fig. 3.3, a capacitor filter is connected across the secondary of the transformer, i.e., on the high voltage side of the transformer. This prevents switching frequency harmonics from entering the system. Also the leakage reactance of the transformer can be used to aid the filtering characteristic. The main drawback of this

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system is that the direct connection of VSI to the transformer primary results in losses in the transformer. The high frequency flux variation causes significant increase in transformer iron losses. To avoid this, a switch frequency LC filter is placed in the transformer primary, i.e., on the inverter side, as shown in Fig. 3.4. The secondary of the transformer is directly connected to the feeder. This will constrain the switch frequency harmonics to remain mainly in the primary side of the transformer. Another advantage of the inverter-side filter is that it is on the low-voltage side of the series transformer and is closer to the harmonic source. However, the introduction of the filter inductor causes a voltage drop and phase-angle shift in the inverter output voltage. This can affect the control scheme of the DVR.

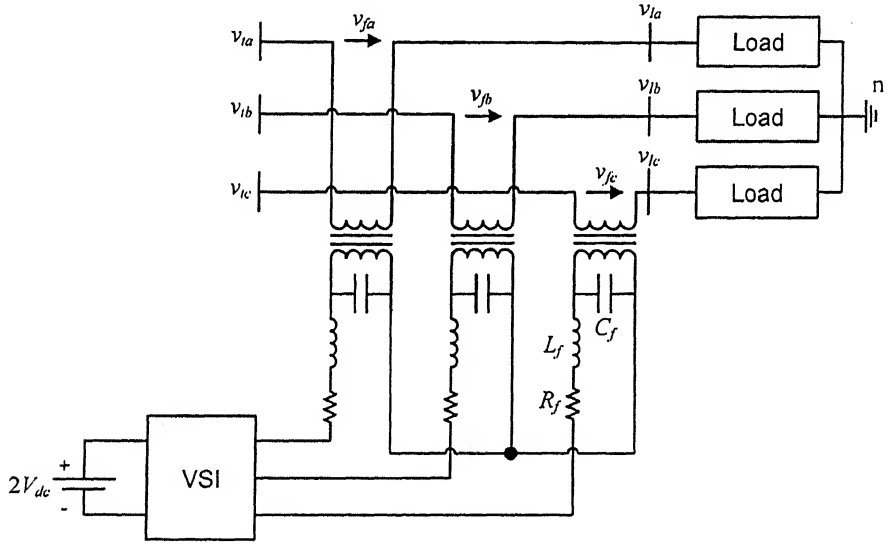

Fig. 3.4 DVR structure with LC filter.

3.3 Generation of Reference Voltages

A single-line diagram of a series compensator connected power system is shown in Fig. 3.5. The series compensator is connected between point of common coupling (PCC) on the left and a load bus (LB) on the right. The instantaneous voltages of the PCC and the load buses are denoted by v_i and v_l respectively. The voltage sources are connected to the series compensator terminals by a feeder with an impedance of $R_s + jX_s$, where $X_s = \omega L_s$, ω being the system fundamental frequency in rad/s. It is assumed that the series compensator is ideal in nature and its voltage is denoted by v_f.

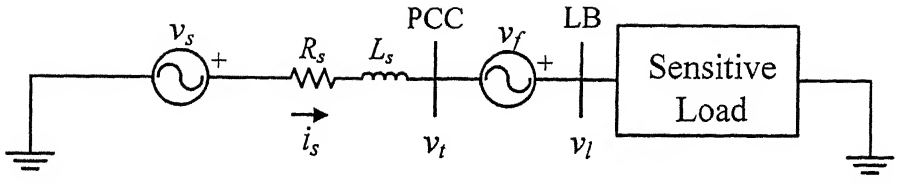

Fig. 3.5 Single-line diagram of a series compensator connected power system.

Using KVL at PCC, we get

$$v_l = v_t + v_f \tag{3.1}$$

It is desired that the DVR regulate the load voltage. The reference voltage of the DVR v_f^* is then given by

$$v_f^* = v_l^* - v_t \tag{3.2}$$

where v_l^* is the desired load voltage. The switches of the VSI of the DVR must now be controlled such that the inverter output voltage v_f closely follows the reference voltage v_f^*.

3.4 Filter Modeling

The filters will introduce some gain as well as phase displacement. So, the reference voltage as calculated in Section 3.3 will need to be modified. Fig. 3.6 shows the single–phase circuit of a series compensated distribution system.

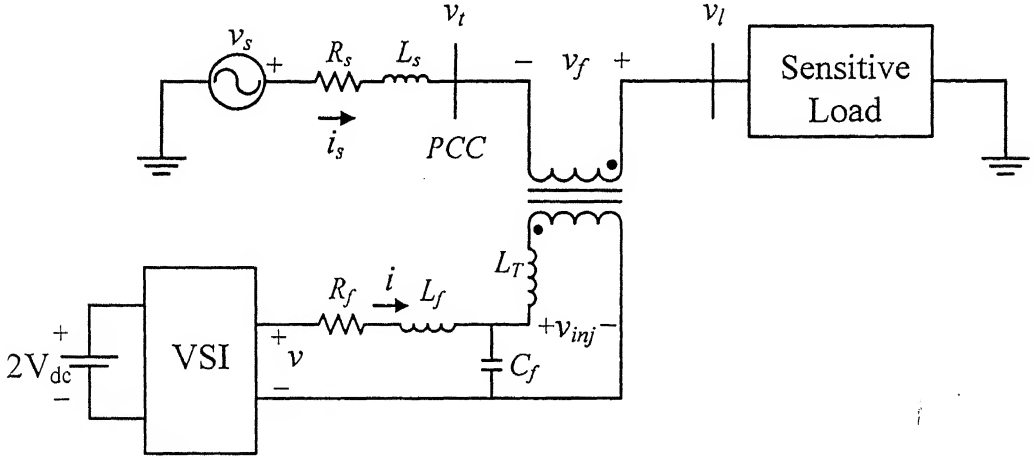

Fig. 3.6 Single-phase circuit of series compensator with LC filter.

The VSI is supported by a dc source and is connected to the system through an LC-filter and a series injection transformer. The injection transformer is assumed to be loss less and having turns ratio of $a = V_p/V_s$, where V_p is the primary voltage (inverter side) and V_s is the secondary voltage (high voltage side). The transformer has a leakage inductance of L_T. The LC filter consists of a series inductor with inductance L_f and resistance R_f and a shunt capacitor with capacitance C_f.

The reference voltage on the primary side of the series injection transformer (v_{inj}^*) is given by,

$$v_{inj}^* = a\left(v_l^* - v_t\right) + \frac{L_T}{a}\frac{di_s}{dt} \tag{3.3}$$

The inverter current i^* can be calculated as,

$$i^* = \frac{i_s}{a} + C_f \frac{dv_{inj}^*}{dt} \tag{3.4}$$

From (3.3) and (3.4) we get,

$$v^* = v_{inj}^* + R_f i^* + L_f \frac{di^*}{dt} \tag{3.5}$$

v^* is the reference voltage for the inverter.

3.5 Simulation Results for DVR Supported by dc Battery

Simulation results of DVR operation for different VSI configurations and space vector techniques are presented in this section for the case when DVR is supported by a dc battery.

3.5.1 Using Two-Level Three-Leg VSI and 2-D SVM

Fig. 3.7 shows the DVR structure with two-level three-leg VSI, which is supported by a dc battery. It is assumed that the source voltages and the load impedances are balanced.

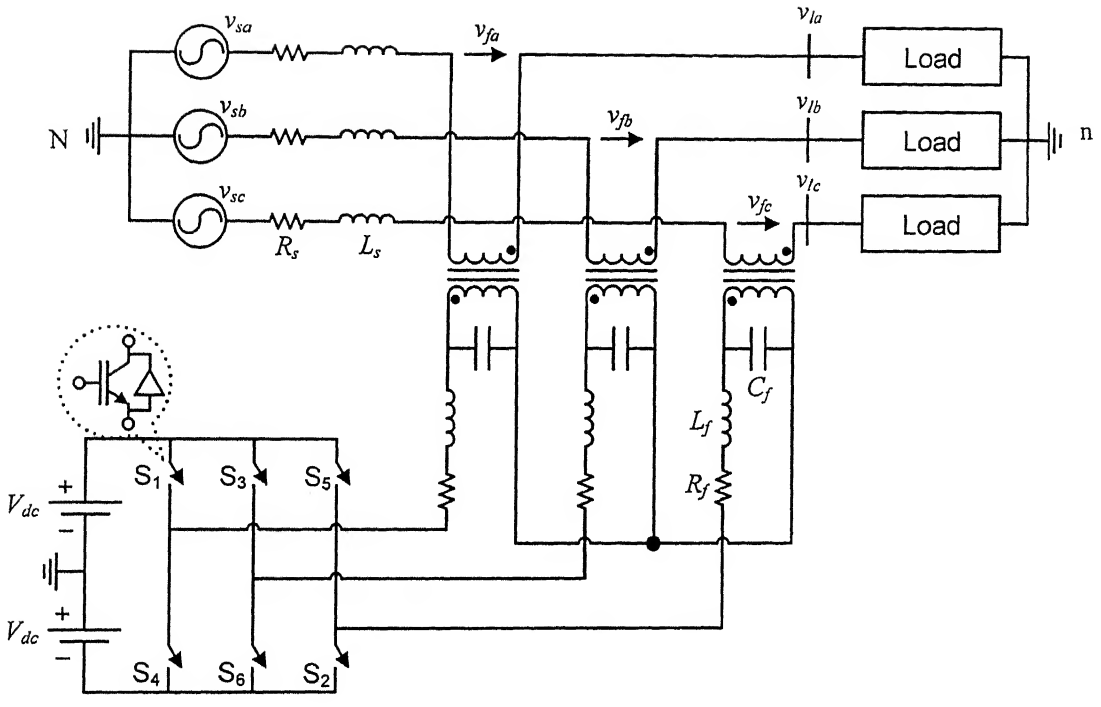

Fig. 3.7 DVR using two-level three-leg VSI with LC filter on inverter side of the isolation transformer.

As the source is balanced, the DVR plays the role only of a voltage regulator in the event of sag and swell and can remove any distortion in the source voltages if they are balanced as well. In case of unbalance in the source voltages, the injected voltages must also be unbalanced. If the injected voltages must be unbalanced, the current injected by the inverter must also be unbalanced. In the Fig. 3.7, the star points of the primary terminals of the three transformers are connected together leaving no path for the zero sequence component of the injected currents to flow. Therefore the DVR cannot compensate for any unbalance in the source voltages.

Three-phase reference voltages for the VSI are calculated using (3.3) to (3.5). These reference voltages are then used to modulate the VSI with 2-D space vector modulation technique as discussed in Section 2.1 [21].

TABLE 3.1

System parameters.

System Frequency	100π rad/s
Source Voltage	11 kV (L-L rms)
Feeder Impedance	$R_s + jX_s = 0.6 + j4.71\ \Omega$
Critical Load	Balanced load of $R_l + jX_l = 148.4 + j67.7\ \Omega$
Filter Parameters	$C_f = 180\ \mu F$, $L_f = 0.5$ mH, $R_f = 2\ \Omega$
Inverter Transformers	Single-phase, 1 MVA, 3.3 kV / 11 kV, 8% leakage reactance
dc bus	$2V_{dc} = 4.0$ kV

The system parameters used for simulation study of Fig. 3.7 are given in Table 3.1. It is desired to keep the load voltages balanced sinusoidal with a peak of 8.96 kV. A three-phase balanced sag of 66% occurs at 0.04 s. The sag lasts for 4 cycles (0.08 s). Fig. 3.8 shows the PCC voltages and the load voltages. It can be notice that the v_l remains almost undisturbed during the sag. As a consequence load currents also remain free of transient as shown in Fig. 3.9 (b). Fig. 3.9 (a) shows the reference voltage and the injected voltage on the primary side of the injection transformer for phase A. It can be seen that the injected voltage follows the reference voltage closely.

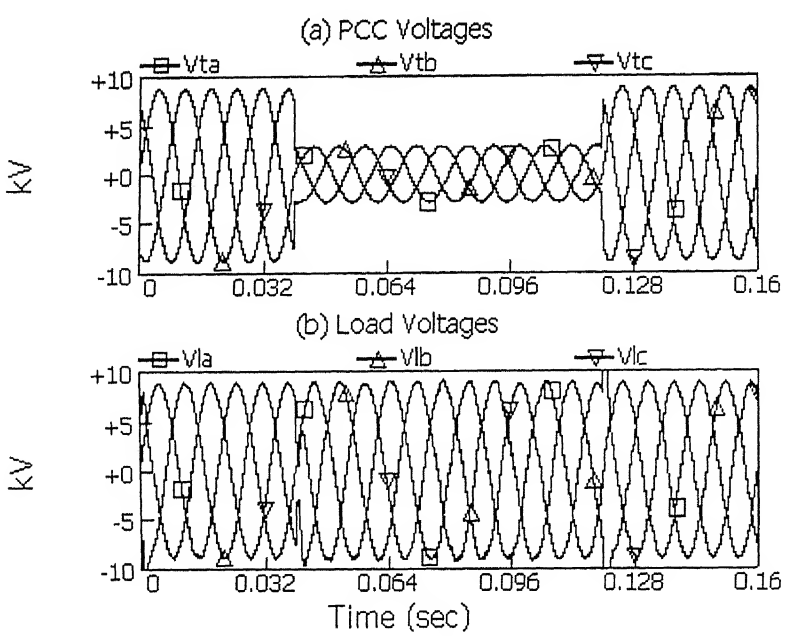

Fig. 3.8 (a) PCC voltages and (b) load voltages during sag with balanced source.

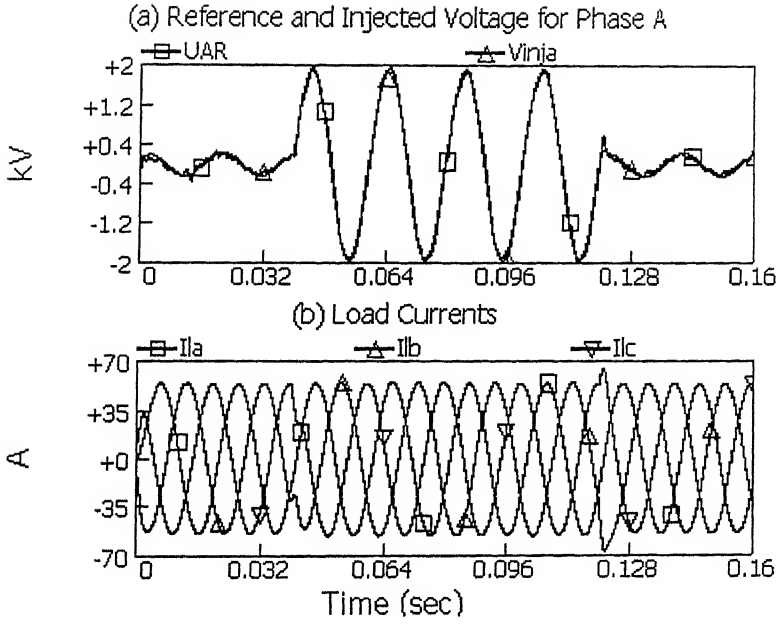

Fig. 3.9 (a) Reference and injected voltage for phase A and (b) Load currents during sag with balanced source.

3.5.2 Using Two-Level Four-Leg VSI and 3-D SVM

The drawback of the DVR realized using two-level three-leg VSI as shown in Fig. 3.7, is that it cannot compensate unbalanced voltages. This is because the star point of the transformer primary is kept isolated and there is no path for neutral current to flow. The DVR realized using neutral clamped VSI could compensate unbalanced voltages. In this scheme the star point of the transformer primary is connected to the middle point of the dc source. However, when SVM, as discussed in Section 2.1, is used as the modulation technique for the VSI of the DVR, the pole voltages contain third harmonic of significant amplitude. Thus, a 2-D SVM modulated neutral clamped VSI cannot be used to realize the DVR.

Fig. 3.10 shows the DVR structure with two-level four-leg VSI, which is supported by a dc battery. Here the star point of the transformer primary is connected to the center point of the fourth leg of the VSI. This connection gives path for zero sequence current to flow. This enables the VSI to inject unbalanced voltages. Since we now have eight switches instead of six, a 3-dimensional space vector technique is used to generate required injection voltages [12]. This has been discussed in Section 2.2.

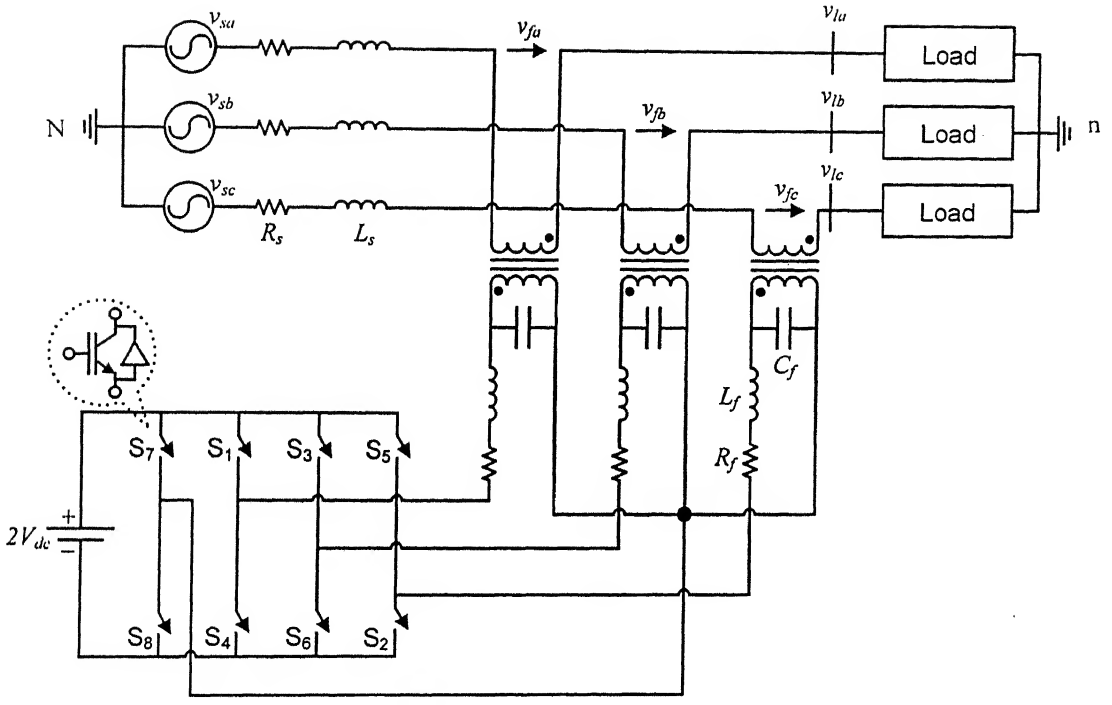

Fig. 3.10 DVR using two-level four-leg VSI with LC filter on inverter side of the isolation transformer.

TABLE 3.2

System parameters.

System Frequency	100π rad/s
Source Voltage	v_{sa} = 1.2*8.965*sin(100 π t) v_{sb} = 0.8*8.965*sin(100πt - 2π/3) v_{sc} = 1.0*8.965*sin(100πt + 2π/3)
Feeder Impedance	$R_s + jX_s = 0.6 + j4.71\ \Omega$
Critical Load	Balanced load of $R_l + jX_l = 148.4 + j67.7\ \Omega$
Filter Parameters	C_f = 120 μF, L_f = 2 mH, R_f = 4.5 Ω
Injection Transformers	Single-phase, 1 MVA, 3.3 kV / 11 kV, 8% leakage reactance
dc bus	$2V_{dc}$ = 3.5 kV

Table 3.2 shows the system parameters used for simulation study of Fig. 3.10 when the source voltages are balanced without any harmonic distortion and the load impedances

are balanced. Balanced three-phase voltage sag of 44% occurs at 0.04 s and it remains for 4 cycles (0.08 s). Simulation results are shown in Fig. 3.11 and Fig. 3.12.

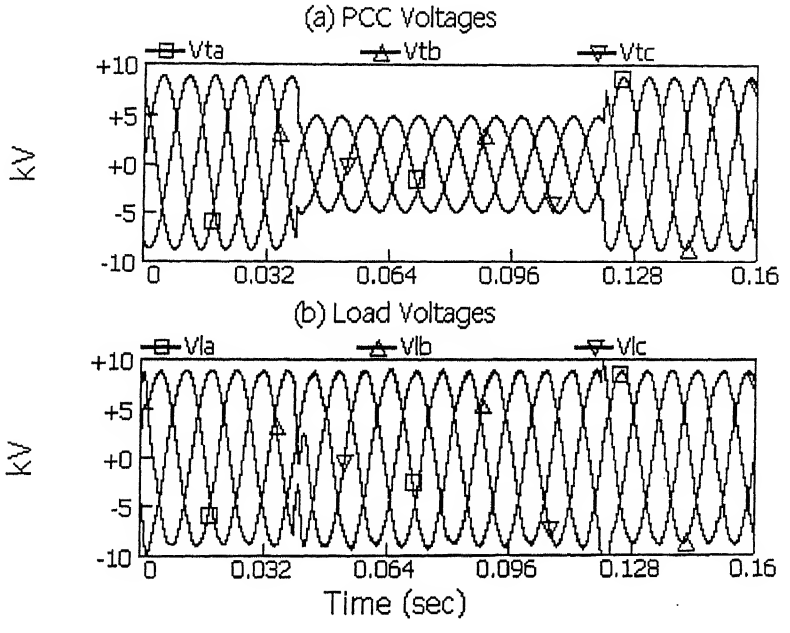

Fig. 3.11 (a) PCC voltages and (b) load voltages during sag with balanced source.

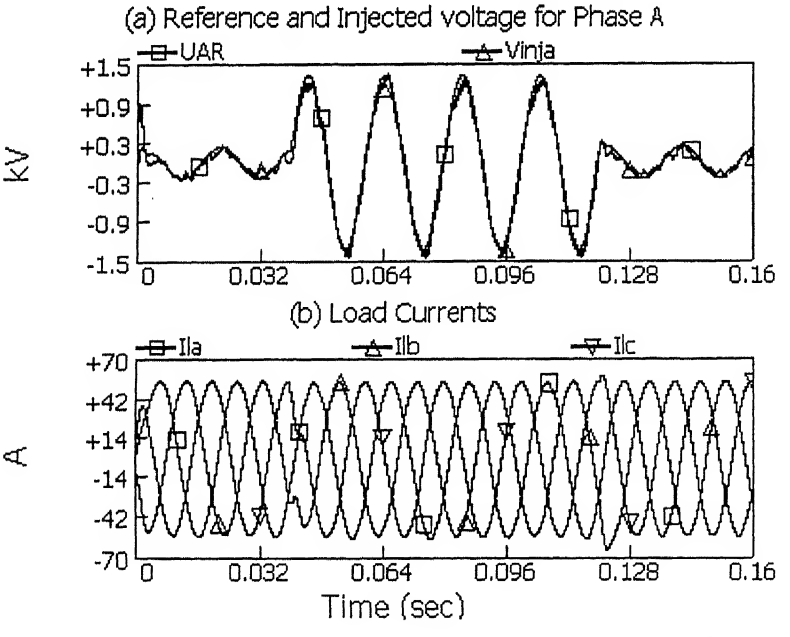

Fig. 3.12 (a) Reference and injected voltage for phase A and (b) Load currents during sag with balanced source.

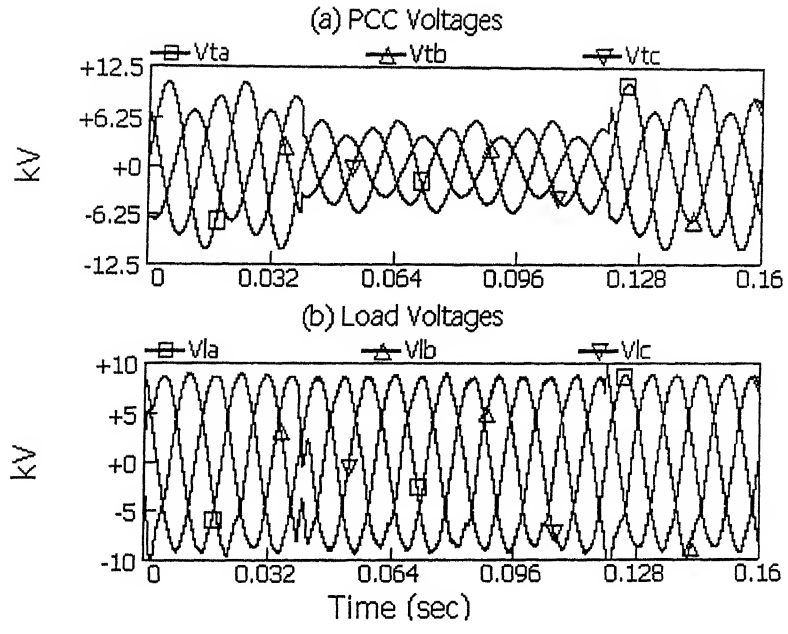

Fig. 3.13 (a) PCC voltages and (b) load voltages during sag with unbalanced source.

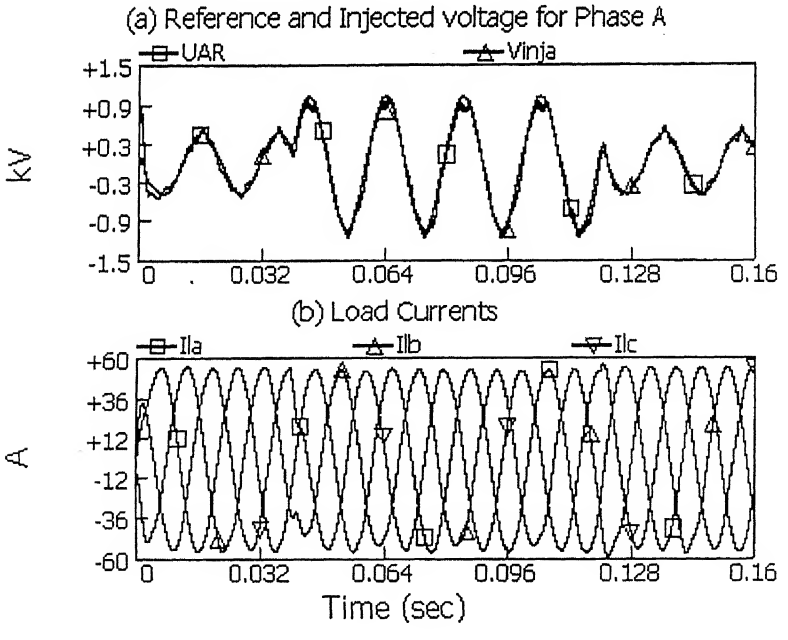

Fig. 3.14 (a) Reference and injected voltages for phase A and (b) Load currents during sag with unbalanced source.

Simulation results for the system of Fig. 3.10 when the source voltages are unbalanced are shown in Fig. 3.13 and Fig. 3.14. The unbalanced source voltages are

$$v_{sa} = 1.2 * 8.965 * \sin(100\pi t)$$

$$v_{sb} = 0.8 * 8.965 * \sin(100\pi t - 2\pi/3)$$

$$v_{sc} = 1.0 * 8.965 * \sin(100\pi t - 4\pi/3)$$

The rest of the parameters chosen for the simulation are as given in Table 3.2.

Voltage sag of 44% occurs at 0.04 s and it remains for 4 cycles (0.08 s). It can be seen that despite the unbalance and voltage sag in the PCC voltages, the load voltages remain balanced throughout.

3.5.3 Using Three Level Diode Clamped VSI and 2-D SVM

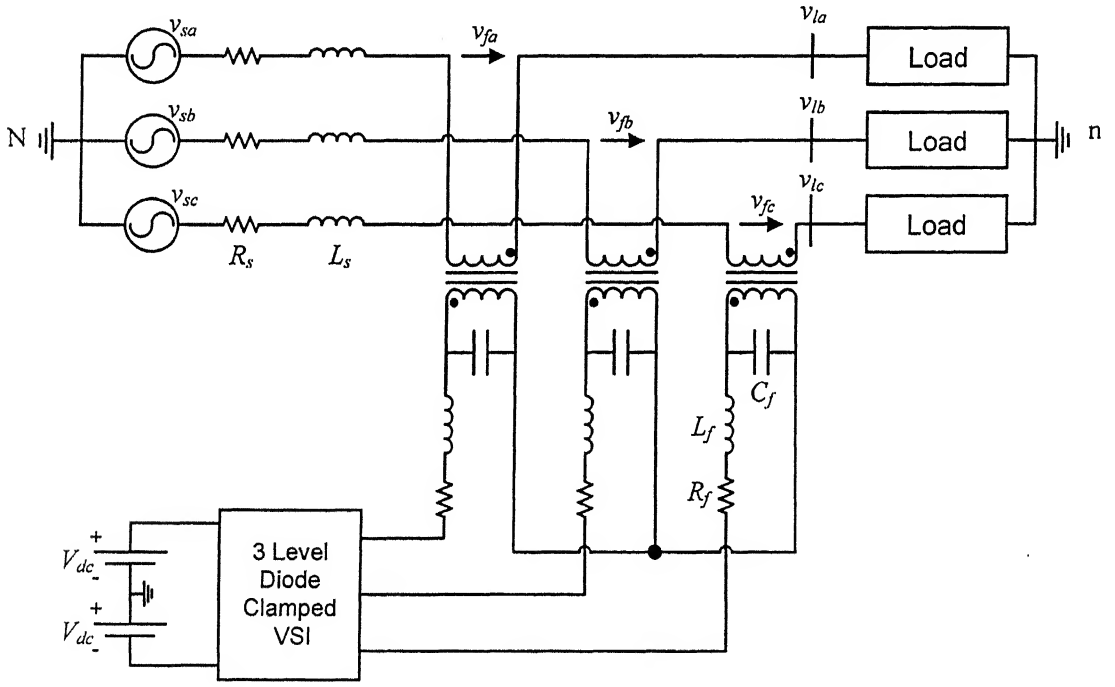

Fig. 3.15 DVR using three-level three-leg VSI with LC filter on inverter side of the isolation transformer.

A DVR using three-level three-leg VSI with LC filter is shown in Fig. 3.15. In this case also the star point of transformer primary is kept isolated. This means no path for neutral current and so this system can only compensate balanced voltage sag or swell.

System parameters for the simulation of Fig. 3.15 are given in Table 3.1. A three-phase balanced sag of 66% occurs at 0.04 s. The sag lasts for 4 cycles (0.08 s). Fig. 3.16 and Fig. 3.17 shows simulation results.

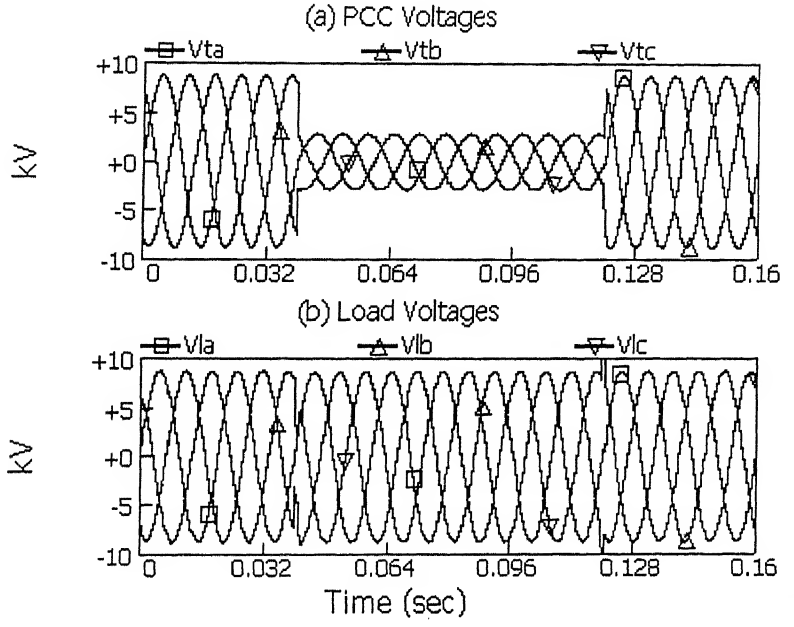

Fig. 3.16 (a) PCC voltages and (b) load voltages during sag with balanced source.

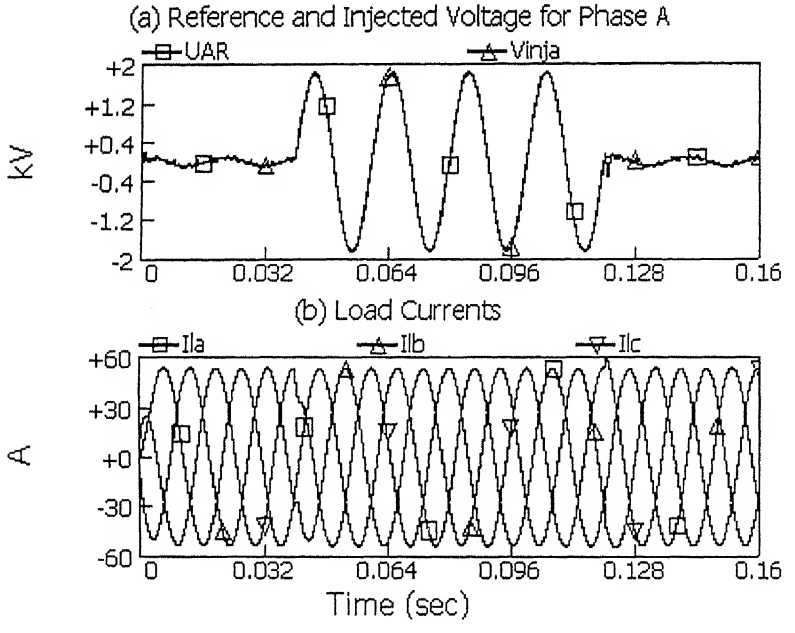

Fig. 3.17 (a) Reference and injected voltage for phase A and (b) Load currents during sag with balanced source.

3.6 Simulation Results for Rectifier Supported DVR

Fig. 3.18 shows single-phase circuit of a system having rectifier supported DVR with LC filter. In this system rectifier is connected to the PCC through a three-phase transformer on ac side. And its dc side is connected to the dc input of the VSI through a dc capacitor. Rectifier takes power from the system and charges the dc capacitor. This capacitor acts as dc source to the VSI.

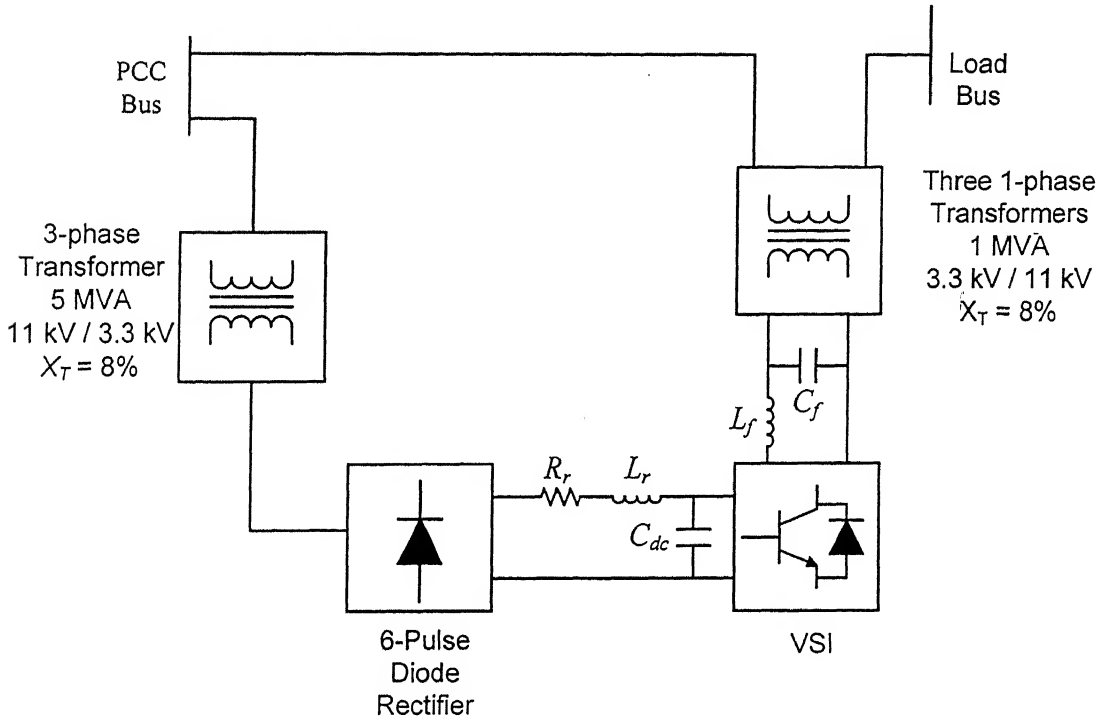

Fig. 3.18 Single-phase circuit of a system having a rectifier supported DVR with LC filter.

Here rectifier acts as a nonlinear load and due to the feeder impedance, the PCC voltages are no longer sinusoidal even though the source voltages are sinusoidal. Parameters chosen for the simulation of this system are given in Table 3.3.

TABLE 3.3

System parameters.

System Frequency	100π rad/s
Source Voltage	11 kV (L-L rms)
Feeder Impedance	$R_s + jX_s = 0.6 + j4.71\ \Omega$
Critical Load	Balanced load of $R_l + jX_l = 148.4 + j67.7\ \Omega$
Filter Parameters	$C_f = 180\ \mu F$, $L_f = 0.5$ mH, $R_f = 2\ \Omega$
Inverter Transformers	Single-phase, 1 MVA, 3.3 kV / 11 kV, 8% leakage reactance
dc link Capacitor	$2V_{dc} = 4.0$ kV
Rectifier Transformer	Three-phase, 5 MVA, 11 kV / 3.3 kV, 8% leakage reactance

A balanced sag of 29% occurs at 0.04 s and it remains for 4 cycles (0.08 s). Fig. 3.19 shows the PCC voltages and load voltages. It can be seen that the PCC voltages are highly distorted while the load voltages are sinusoidal. Fig. 3.20 shows the voltage across capacitor and Fig. 3.21 shows the load currents. Capacitor voltage dips during sag and retains its previous value when sag gets cleared.

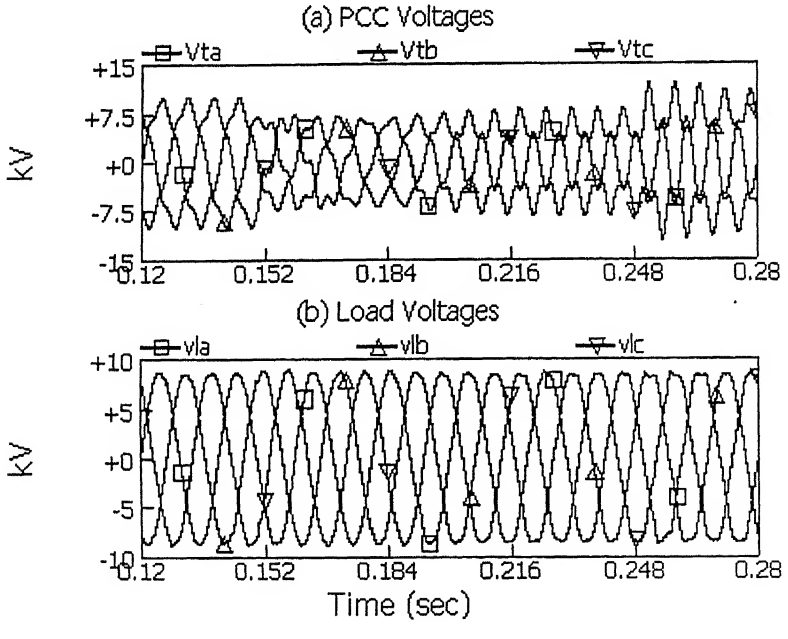

Fig. 3.19 PCC and Load voltages.

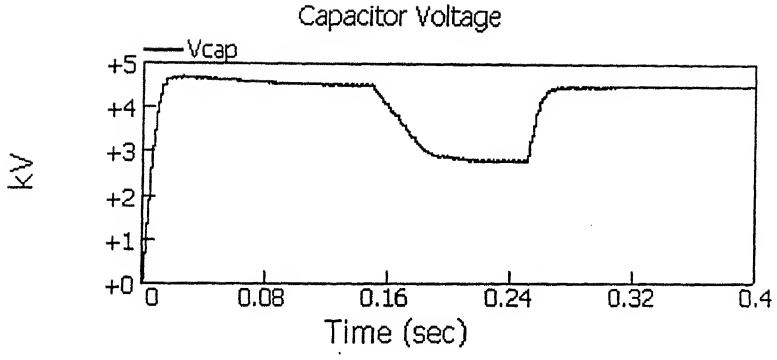

Fig. 3.20 Capacitor Voltage.

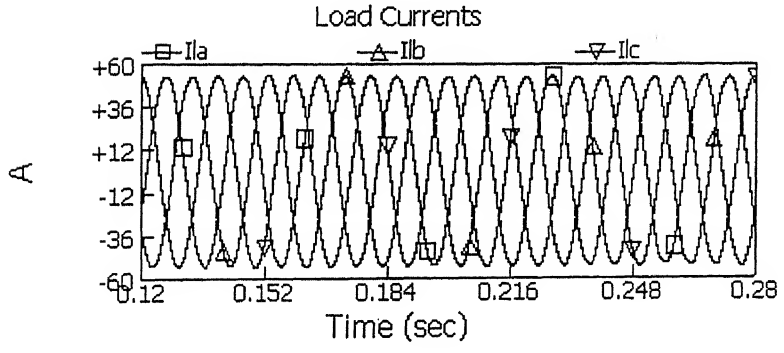

Fig. 3.21 Load currents.

3.7 Performance Comparison of DVR Using Different VSI Configurations

Simulation results of DVR using three different types of VSI are presented in the previous sections. The DVR using two-level three-leg VSI and three-level diode clamped VSI can compensate balanced voltage sag/swell but it cannot compensate unbalanced sag/swell. This is because the star point of the transformer primary is kept isolated and there is no path for zero sequence current to flow. 2-D SVM techniques were used for modulating VSIs.

The DVR using two-level four-leg VSI and 3-D SVM can compensate for balanced as well as unbalanced sag/swell. But it requires one additional leg and 3-D SVM technique has to be used, which is complicated compared to 2-D SVM.

Table 3.4 shows the comparisons of three VSI topologies using which DVR has been realized.

TABLE 3.4

Comparison of DVR realized using different VSI topologies.

Topology of the VSI used	No. of Switches	Comments
Two-level three-leg VSI (Fig. 3.7)	6	It uses the least number of switches. It however can compensate only for the balanced disturbances on the supply side. A simple two dimensional space vector modulation technique can be used for this VSI. The use of SVM technique results in the increase of modulation index by 15 %.
Two-level four-leg VSI (Fig. 3.10)	8	It uses two more switches compared to two-level three-leg VSI. The star point of the injection transformer primary is connected to the middle point of the fourth leg. This connection provides path for the zero sequence current. It can compensate for balanced as well as unbalanced disturbances on the supply side. A three-dimensional SVM technique is to be used for this VSI.
Three-level diode-clamped VSI (Fig. 3.15)	12	It uses twelve switches. The voltage stress across each switch reduces by 50% compared to the switches of a two level VSI with the same dc link voltage. So, the higher power rating can be achieved using the same switches. This topology can also compensate only balanced disturbances on the supply side. A multilevel SVM problem can be reduced to that of a two-level SVM problem and then it can be implemented in the same way as a two-level SVM.

CHAPTER 4

CONCLUSIONS

The general conclusions drawn from the thesis and scope for the future work is presented in this chapter.

4.1 Conclusions

1. When the VSI is modulated using SVM, the amplitude modulation index can be increased by 15% compared to the SPWM. That means the rating of the dc link voltage required can be reduced by 15%.
2. In two-level three-leg VSI and three-level diode clamped VSI, the pole voltages, i.e., voltages of output terminals with respect to the middle point of the dc source, contains third harmonic when the VSI is modulated using SVM.
3. The placement and the choice of zero vectors are not fixed for SVM and different switching sequences can be implemented to achieve required harmonic and switching performances.
4. For three-level diode clamped VSI, a technique in which the three-level SVM problem simplifies to that of a two-level SVM problem has been implemented.
5. DVR realized using two-level three-leg VSI and three-level diode clamped VSI separately, can compensate balanced voltage sag/swell.
6. The rectifier supported DVR realized using three-level diode clamped VSI compensates voltage sag/swell. During the voltage sag/swell disturbance the capacitor voltage dips and settles at a lower value and retains its original value when the disturbance is cleared.
7. For two-level four-leg VSI there are sixteen switching vectors, which are distributed in 3-dimensional space. Thus, a 3-D SVM technique has to be used for this VSI.
8. The DVR realized using two-level four-leg VSI has the capability to inject unbalanced voltages as the connection from the star point of the transformer

primary to the middle point of the fourth leg gives path for zero sequence current to flow.

4.2 Scope for Future Work

Some suggestions for the future work are

1. 3-D SVM can be implemented for multi-level VSI.
2. DVR can be supported by capacitors only, where the capacitors will be charged thorough the VSI it is supporting.

Appendix A

TABLE A.1

Projection Matrices for 3-D SVM

Prism	Projection Matrices for Tetrahedrons			
1	T_1 $\begin{bmatrix} \frac{4}{3} & 0 & \frac{2}{3} \\ \frac{4}{3} & 0 & -\frac{4}{3} \\ \frac{2}{3} & \frac{2}{\sqrt{3}} & -\frac{2}{3} \end{bmatrix}$	T_2 $\begin{bmatrix} \frac{4}{3} & 0 & \frac{2}{3} \\ \frac{2}{3} & \frac{2}{\sqrt{3}} & \frac{4}{3} \\ \frac{2}{3} & \frac{2}{\sqrt{3}} & -\frac{2}{3} \end{bmatrix}$	T_{13} $\begin{bmatrix} 0 & 0 & -2 \\ \frac{4}{3} & 0 & -\frac{4}{3} \\ \frac{2}{3} & \frac{2}{\sqrt{3}} & -\frac{2}{3} \end{bmatrix}$	T_{14} $\begin{bmatrix} \frac{4}{3} & 0 & \frac{2}{3} \\ \frac{2}{3} & \frac{2}{\sqrt{3}} & \frac{4}{3} \\ 0 & 0 & 2 \end{bmatrix}$
2	T_3 $\begin{bmatrix} -\frac{2}{3} & \frac{2}{\sqrt{3}} & \frac{2}{3} \\ \frac{2}{3} & \frac{2}{\sqrt{3}} & \frac{4}{3} \\ \frac{2}{3} & \frac{2}{\sqrt{3}} & -\frac{2}{3} \end{bmatrix}$	T_4 $\begin{bmatrix} -\frac{2}{3} & \frac{2}{\sqrt{3}} & \frac{2}{3} \\ -\frac{2}{3} & \frac{2}{\sqrt{3}} & -\frac{4}{3} \\ \frac{2}{3} & \frac{2}{\sqrt{3}} & -\frac{2}{3} \end{bmatrix}$	T_{15} $\begin{bmatrix} 0 & 0 & -2 \\ -\frac{2}{3} & \frac{2}{\sqrt{3}} & -\frac{4}{3} \\ \frac{2}{3} & \frac{2}{\sqrt{3}} & -\frac{2}{3} \end{bmatrix}$	T_{16} $\begin{bmatrix} -\frac{2}{3} & \frac{2}{\sqrt{3}} & \frac{2}{3} \\ \frac{2}{3} & \frac{2}{\sqrt{3}} & \frac{4}{3} \\ 0 & 0 & 2 \end{bmatrix}$
3	T_5 $\begin{bmatrix} -\frac{2}{3} & \frac{2}{\sqrt{3}} & \frac{2}{3} \\ -\frac{2}{3} & \frac{2}{\sqrt{3}} & -\frac{4}{3} \\ -\frac{4}{3} & 0 & -\frac{2}{3} \end{bmatrix}$	T_6 $\begin{bmatrix} -\frac{2}{3} & \frac{2}{\sqrt{3}} & \frac{2}{3} \\ -\frac{4}{3} & 0 & \frac{4}{3} \\ -\frac{4}{3} & 0 & -\frac{2}{3} \end{bmatrix}$	T_{17} $\begin{bmatrix} 0 & 0 & -2 \\ -\frac{2}{3} & \frac{2}{\sqrt{3}} & -\frac{4}{3} \\ -\frac{4}{3} & 0 & -\frac{2}{3} \end{bmatrix}$	T_{18} $\begin{bmatrix} -\frac{2}{3} & \frac{2}{\sqrt{3}} & \frac{2}{3} \\ -\frac{4}{3} & 0 & \frac{4}{3} \\ 0 & 0 & 2 \end{bmatrix}$
4	T_7 $\begin{bmatrix} -\frac{2}{3} & -\frac{2}{\sqrt{3}} & \frac{2}{3} \\ -\frac{4}{3} & 0 & \frac{4}{3} \\ -\frac{4}{3} & 0 & -\frac{2}{3} \end{bmatrix}$	T_8 $\begin{bmatrix} -\frac{2}{3} & -\frac{2}{\sqrt{3}} & \frac{2}{3} \\ -\frac{2}{3} & -\frac{2}{\sqrt{3}} & -\frac{4}{3} \\ -\frac{4}{3} & 0 & -\frac{2}{3} \end{bmatrix}$	T_{19} $\begin{bmatrix} 0 & 0 & -2 \\ -\frac{2}{3} & -\frac{2}{\sqrt{3}} & -\frac{4}{3} \\ -\frac{4}{3} & 0 & -\frac{2}{3} \end{bmatrix}$	T_{20} $\begin{bmatrix} -\frac{2}{3} & -\frac{2}{\sqrt{3}} & \frac{2}{3} \\ -\frac{4}{3} & 0 & \frac{4}{3} \\ 0 & 0 & 2 \end{bmatrix}$
5	T_9 $\begin{bmatrix} -\frac{2}{3} & -\frac{2}{\sqrt{3}} & \frac{2}{3} \\ -\frac{2}{3} & -\frac{2}{\sqrt{3}} & -\frac{4}{3} \\ \frac{2}{3} & -\frac{2}{\sqrt{3}} & -\frac{2}{3} \end{bmatrix}$	T_{10} $\begin{bmatrix} -\frac{2}{3} & -\frac{2}{\sqrt{3}} & \frac{2}{3} \\ \frac{2}{3} & -\frac{2}{\sqrt{3}} & \frac{4}{3} \\ \frac{2}{3} & -\frac{2}{\sqrt{3}} & -\frac{2}{3} \end{bmatrix}$	T_{21} $\begin{bmatrix} 0 & 0 & -2 \\ -\frac{2}{3} & -\frac{2}{\sqrt{3}} & -\frac{4}{3} \\ \frac{2}{3} & -\frac{2}{\sqrt{3}} & -\frac{2}{3} \end{bmatrix}$	T_{22} $\begin{bmatrix} -\frac{4}{3} & 0 & \frac{2}{3} \\ \frac{2}{3} & \frac{2}{\sqrt{3}} & \frac{4}{3} \\ 0 & 0 & 2 \end{bmatrix}$
6	T_{11} $\begin{bmatrix} \frac{4}{3} & 0 & \frac{2}{3} \\ \frac{4}{3} & 0 & -\frac{4}{3} \\ \frac{2}{3} & \frac{2}{\sqrt{3}} & -\frac{2}{3} \end{bmatrix}$	T_{12} $\begin{bmatrix} -\frac{2}{3} & \frac{2}{\sqrt{3}} & \frac{2}{3} \\ -\frac{2}{3} & \frac{2}{\sqrt{3}} & -\frac{4}{3} \\ \frac{2}{3} & \frac{2}{\sqrt{3}} & -\frac{2}{3} \end{bmatrix}$	T_{23} $\begin{bmatrix} 0 & 0 & -2 \\ \frac{4}{3} & 0 & -\frac{4}{3} \\ \frac{2}{3} & \frac{2}{\sqrt{3}} & -\frac{2}{3} \end{bmatrix}$	T_{24} $\begin{bmatrix} \frac{4}{3} & 0 & \frac{2}{3} \\ \frac{2}{3} & \frac{2}{\sqrt{3}} & \frac{4}{3} \\ 0 & 0 & 2 \end{bmatrix}$

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